Adapt-A-Link Family
Converters and Repeaters

User's Manual

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Chapter 1 - Introduction

Introduction

This chapter outlines the key features of the Adapt-A-Link adapters family.

The family consists of the following 11 members:

Repeaters:

CLCL	Full Camera Link Repeater
LVLV	LVDS Repeater

Converters:

DVICL	DVI-to-Camera Link Converter
BCL	Base Camera Link to LVDS Converter
MCL	Medium Camera Link to LVDS Converter
BCR	Base Camera Link to RS422 Converter
MCR	Medium Camera Link to RS422 Converter
BRC	RS422 to Base Camera Link Converter
MRC	RS422 to Medium Camera Link Converter
BLC	LVDS to Base Camera Link Converter
MLC	LVDS to Medium Camera Link Converter

1.1 General Description

Camera Link is a communications interface developed for use in vision applications. The specification for the Camera Link interface was developed by a group of industrial camera and frame grabber manufacturers. The Camera Link specification is an open structure, which gives manufacturers the ability to differentiate their products while maintaining interface compatibility. In the past, the industrial digital video market had lacked a standard method of communication between the cameras and frame grabbers. Since Camera Link is a relatively new standard, many current digital video camera manufacturers use LVDS communication as specified for RS644. Although RS644 is an improvement over older methods utilizing differential signals for communication, such as RS422, there are still many cameras in production and on the market using RS422. The major obstacle for the users of these cameras is the frame grabber interface, where different frame grabbers, not compatible with each other, are needed for the different camera interface standards.

To overcome this obstacle, **IMPERX** has developed a series of interface adapters, the Adapt-A-Link family, which convert the interface signals from cameras using DVI, LVDS (RS644) and RS422 standards to a set of signals fully compatible to the Base or Medium configuration Camera Link interface. The adapters also convert Base or Medium configuration Camera Link interface to LVDS (RS644) and RS422 standards, so legacy frame grabber can be used with new cameras. Thus, all available DVI, LVDS, RS422, and Camera Link digital cameras on the market can be interfaced to all available LVDS, RS422, and Camera Link frame grabbers – Figure 1. The adapters cover a wide range of data signal configurations, camera enable signals, camera control signals, data clocks and asynchronous RS232 serial communication. Adapt-A-Link technical specifications are shown in Table 1. Each adapter is designed as a stand-alone unit with autonomous power supply.

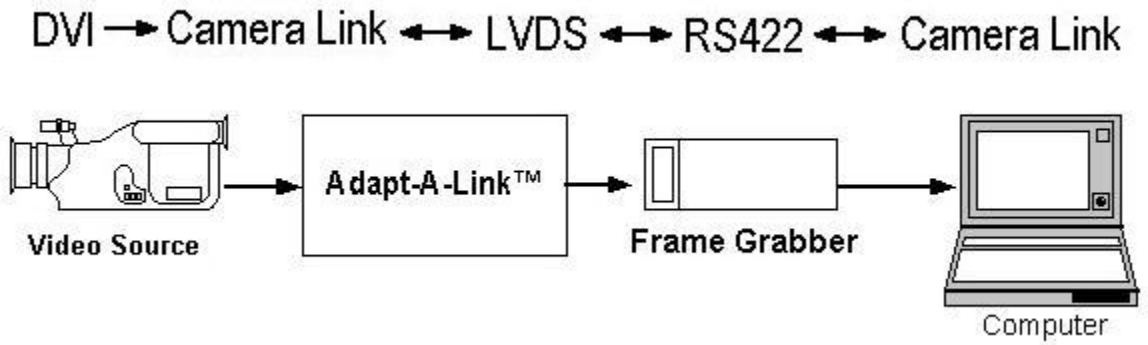

Figure 1. Adapt-A-Link Connectivity.

1.2 Technical Specifications

CLCL - Camera Link Repeater - Full Camera Link Extender	
Input	Full Camera Link
Output	Full Camera Link
Clock	85 MHz Max.
Power	6.0 VDC, 300 mA
Dimensions	5.0" x 3.0" x 1.5"

LVLV - LVDS Repeater - LVDS to LVDS Extender	
Input	32 LVDS data inputs 4 LVDS enable inputs 4 LVDS control outputs 1 LVDS data clock 1 RS232 serial interface
Output	32 LVDS data outputs 4 LVDS enable outputs 4 LVDS control inputs 1 LVDS data clock 1 RS232 serial interface
Clock	66 MHz max
Power	6.0 VDC, 300 mA
Dimensions	5.0" x 3.0" x 1.5"

DVICL - DVI digital video input to Camera Link video output	
Input	DVI - D
Resolution	VGA (640 x 480) to UXGA (1600 x 1200)
Output	Dual Base Camera Link
Clock	Data clock - 82.5 MHz Max
Power	6.0 VDC, 300 mA
Dimensions	5.0" x 3.0" x 1.5"

BCL - Base Camera Link to LVDS (RS644) Interface	
Input	Base Camera Link
Output	24 LVDS data outputs 4 LVDS enable outputs 4 LVDS control inputs 1 LVDS data clock 1 RS232 serial interface
Clock	66 MHz max
Power	6.0 VDC, 300 mA
Dimensions	5.0" x 3.0" x 1.5"

MCL - Medium Camera Link to LVDS (RS644) Interface	
Input	Medium Camera Link
Output	48 LVDS data outputs 8 LVDS enable outputs 4 LVDS control inputs 1 LVDS data clock 1 RS232 serial interface
Clock	66 MHz max
Power	6.0 VDC, 500 mA
Dimensions	5.0" x 3.0" x 1.5"

BCR - Base Camera Link to RS422 Interface	
Input	Base Camera Link
Output	24 RS422 data outputs 4 RS422 enable outputs 4 RS422 control inputs 1 RS422 data clock 1 RS232 serial interface
Clock	33 MHz max
Power	6.0 VDC, 600 mA
Dimensions	5.0" x 3.0" x 1.5"

MCR - Medium Camera Link to RS422 Interface	
Input	Medium Camera Link
Output	48 RS422 data outputs 8 RS422 enable outputs 4 RS422 control inputs 1 RS422 data clock 1 RS232 serial interface
Clock	33 MHz max
Power	6.0 VDC, 1000 mA
Dimensions	5.0" x 3.0" x 1.5"

BRC - RS422 to Base Camera Link Interface	
Input	24 RS422 data inputs 4 RS422 enable inputs 4 RS422 control outputs 1 RS422 data clock 1 RS232 serial interface
Output	Base Camera Link
Clock	33 MHz max
Power	6.0 VDC 300 mA
Dimensions	5.0" x 3.0" x 1.5"

MRC - RS422 to Medium Camera Link Interface	
Input	48 RS422 data inputs 8 RS422 enable inputs 4 RS422 control outputs 1 RS422 data clock 1 RS232 serial interface
Output	Medium Camera Link
Clock	33 MHz max
Power	6.0 VDC, 500 mA
Dimensions	5.0" x 3.0" x 1.5"

BLC - LVDS (RS644) to Base Camera Link Interface	
Input	24 LVDS data inputs 4 LVDS enable inputs 4 LVDS control outputs 1 LVDS data clock 1 RS232 serial interface
Output	Base Camera Link
Clock	66 MHz max
Power	6.0 VDC, 300 mA
Dimensions	5.0" x 3.0" x 1.5"

MLC - LVDS (RS644) to Medium Camera Link Interface	
Input	48 LVDS data inputs 8 LVDS enable inputs 4 LVDS control outputs 1 LVDS data clock 1 RS232 serial interface
Output	Medium Camera Link
Clock	66 MHz max
Power	6.0 VDC, 500 mA
Dimensions	5.0" x 3.0" x 1.5"

Chapter 2 – Adapt-A-Link Features

Adapt-A-Link Features

This chapter discusses the adapters features and their use.

2.1 DVICL – DVI to Camera Link Converter

DVICL is designed to interface any standard DVI digital source to any standard Camera Link frame grabber. It converts the standard digital DVI interface signals to a standard Base (or dual Base) configuration Camera Link output interface – Figure 2. DVICL supports resolutions from VGA (640 x 480) pixels to UXGA (1600 x 1200) pixels including HD (1920 x 1080) pixels. The maximum data clock is 82.5 MHz. Figure 3 shows back and front views of the DVICL. Table 1 describes the pin assignments for DVI interface. Table 2 describes the supported video resolutions and the corresponding data rates. Detailed views of the DVI input and Camera link output connectors are shown in Appendix 1.

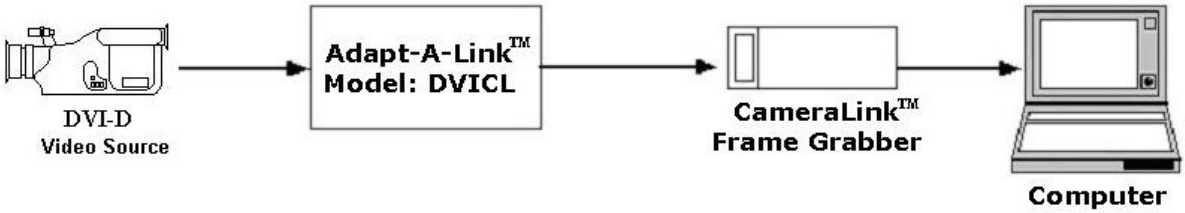

Figure 2. DVICL Connectivity

Figure 3. DVICL front (top) and back (bottom) views.

PIN	DVI Signal Name
1	T.M.D.S. Data 2 -
2	T.M.D.S. Data 2 +
3	T.M.D.S. Data 2/4 Shield
4	T.M.D.S. Data 4 -
5	T.M.D.S. Data 4+
6	DDC Clock
7	DDC Data
8	N/C
9	T.M.D.S. Data 1 -
10	T.M.D.S. Data 1 +
11	T.M.D.S. Data 1/3 Shield
12	T.M.D.S. Data 3 -
13	T.M.D.S. Data 3 +
14	+ 5.0 VDC Power
15	Ground (for 5.0 VDC)
16	Hot Plug Detect
17	T.M.D.S. Data 0 -
18	T.M.D.S. Data 0 +
19	T.M.D.S. Data 0/5 Shield
20	T.M.D.S. Data 5 -
21	T.M.D.S. Data 5 +
22	T.M.D.S. Clock Shield +
23	T.M.D.S. Clock +
24	T.M.D.S. Clock 5 -

Table 1. Pin assignments for DVI interface.

Video Format	Horiz. Pixels	Vertical Lines	Refresh Rate (Hz)	Overhead	Pixel Rate Mpix/sec	Data Rate Mb/sec	DVI-CL Output	Camera Link Clock (MHz)
VGA	640	480	60	1.3	24	719	Base	24
VGA	640	480	70	1.3	28	839	Base	28
VGA	640	480	80	1.3	31.9	958	Base	31.9
VGA	640	480	90	1.3	35.9	1078	Base	35.9
VGA	640	480	100	1.3	39.9	1198	Base	39.9
SVGA	800	600	60	1.3	37.4	1123	Base	37.4
SVGA	800	600	70	1.3	43.7	1310	Base	43.7
SVGA	800	600	80	1.3	49.9	1498	Base	49.9
SVGA	800	600	90	1.3	56.2	1685	Base	56.2
SVGA	800	600	100	1.3	62.4	1872	Base	62.4
XGA	1024	768	60	1.3	61.3	1840	Base	61.3
XGA	1024	768	70	1.3	71.6	2147	Base	71.6
XGA	1024	768	80	1.3	81.8	2454	Base	81.8
XGA	1024	768	90	1.3	92.0	2760	Dual Base	46.0
XGA	1024	768	100	1.3	102.2	3067	Dual Base	51.1
SXGA	1280	1024	60	1.3	102.2	3067	Dual Base	51.1
SXGA	1280	1024	70	1.3	119.3	3578	Dual Base	59.6
SXGA	1280	1024	80	1.3	136.3	4089	Dual Base	68.2
SXGA	1280	1024	90	1.3	153.4	4601	Dual Base	76.7
SXGA	1280	1024	100	1.3	170.4	5112	Dual Base	85.2
UXGA	1600	1200	60	1.3	149.8	4493	Dual Base	74.9
UXGA	1600	1200	70	1.3	174.7	5242	2x Dual Base	43.7
UXGA	1600	1200	80	1.3	199.7	5990	2x Dual Base	49.9
UXGA	1600	1200	90	1.3	224.6	6739	2x Dual Base	56.2
UXGA	1600	1200	100	1.3	249.6	7488	2x Dual Base	62.4
HD	1920	1080	30	1.3	80.9	2426	Base	80.9
HD	1920	1080	60	1.3	161.7	4852	Dual Base	80.9
QXGA	2048	1536	30	1.3	122.7	3681	Dual Base	61.3
QXGA	2048	1536	60	1.3	245.4	7361	2x Dual Base	61.4

Table 2. DVI-CL Supported video resolution and data rates.

NOTES:

1. Pixel Rate, Data Rate and CL Clock numbers may vary slightly depending on type of signal source. Overhead is source dependent.
2. DVI Input Data Rate: 165 MPix/sec (single TMDS link limit). This sets the upper limit of operation at UXGA (1600 x 1200) @ 60 Hz
3. Camera Link Output Clock: 25 MHz minimum, 82.5 MHz maximum (Camera Link Transmitter limitation), This sets the low end of operation at VGA (640 x 480) @ >60 Hz.
4. RED LED: Illuminated when unit is operating in " Dual Output Mode", controlled by "Mode" switch.
5. Mode Switch: Switches operating mode between Single and Dual output mode:

   a. UP Position: Dual output mode, red led "on"
   b. DOWN Position: Single output mode, red led "off"
6. Sync Polarity Switch: Inverts horizontal and vertical sync signals. Correct H/V-Sync Polarity is resolution and source dependent and needs to be determined in the actual configuration.
   a. UP Position: Inverting mode
   b. DOWN Position: Non Inverting mode
7. CL Single Output:
   a. Odd & Even pixels in "Base" mode
   b. Even pixels in “Dual” mode
8. Dual Output:
   a. No signals in "Single" mode,
   b. Odd pixels in "Dual" mode
9. GREEN LED: illuminated when internal supply voltage is normal, unit is ready for operation

OPERATING INSTRUCTIONS:

1. Connect AC-DC adaptor to DVI-CL converter. Green LED should be on.
2. Connect DVI source to DVI input through DVI cable (not supplied).
3. Connect Camera Link output to input of receiving device using one or two Camera Link cables depending on configuration:
   a. For VGA (640 x 480), SVGA (800 x 600) and XGA (1024 x 768) up to 60 Hz use Base Camera Link mode (single output),
   b. For XGA (1024 x 768) @ 60 Hz, SXGA (1280 x 1024) and UXGA (1600 x 1200) @ 60 Hz use dual Base Camera Link mode (dual output). **Note:** This mode is different from standard medium/full Camera Link mode.
4. For dual output mode the even pixel are present on "single" connector, the odd pixels are present on "dual" connector.
5. Because of the wide range of possible input devices (example PC video card), the horizontal/vertical sync. polarity may vary. Therefore a switch has been provided so that the converter can be configured to match the source signal. The correct setting cannot be predicted accurately but has to be determined after the signal chain is set up. If sync polarity is incorrect, image will be black, unstable or corrupted. In this case the opposite setting should give a stable image.
6. If input signal requires dual output mode switch unit to "dual" mode (switch in "up" position, red led "on").
7. Power requirements – 6.0 VDC, 300 mA.

Common problems:

1. The unit has no power due to loose DC connector or lack of AC. Check green LED.
2. If the unit generates an output signal but image is corrupted or unstable switch sync polarity. If this does not resolve the problem, input signal bandwidth may be:
   a. Too high for single output mode, use dual output mode,
   b. Below minimum Camera Link clock rate, increase pixel/refresh rate.

2.2 CLCL – Camera Link Repeater

CLCL is a Full Camera Link repeater (10 meter extender), designed to extend the distance between any high-resolution digital Camera Link camera and any standard Camera Link frame grabber by 10 meters (30 feet). It reconditions and converts the standard Full configuration Camera Link input interface signals to a standard Full configuration Camera Link output interface – Figure 4. CLCL supports 64 data signals (72 total, or up to 80 data signals with multiplexing data and enable signals), 4 control signals, 12 enable signals, three data clock signals, and one RS232 serial interface. The maximum data clock is 85 MHz. Figure 5 shows back and front views of the CLCL. Table 3 (a, b) describes the pin assignments for the 26 pin Camera Link input connectors. Table 4 (a, b) describes the pin assignments for the 26 pin Camera Link output connectors. Detailed views of the Camera link connectors are shown in Appendix 1.

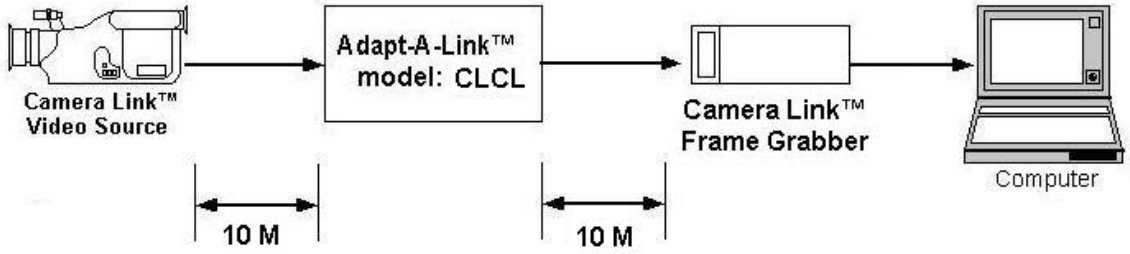

Figure 4. CLCL Connectivity

Figure 5. CLCL front (top) and back (bottom) views.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- X 0	- PAIR 1
12	+ X 0	+ PAIR 1
24	- X 1	- PAIR 2
11	+ X 1	+ PAIR 2
23	- X 2	- PAIR 3
10	+ X 2	+ PAIR 3
22	- X CLK	- PAIR 4
9	+ X CLK	+ PAIR 4
21	- X 3	- PAIR 5
8	+ X 3	+ PAIR 5
20	+ SerTC	+ PAIR 6
7	- SerTC	- PAIR 6
19	- SerTFG	- PAIR 7
6	+ SerTFG	+ PAIR 7
18	- CC 1	- PAIR 8
5	+ CC 1	+ PAIR 8
17	+ CC 2	+ PAIR 9
4	- CC 2	- PAIR 9
16	- CC 3	- PAIR 10
3	+ CC 3	+ PAIR 10
15	+ CC 4	+ PAIR 11
2	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 3a. Pin assignments for the first (Base) 26 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- Y 0	- PAIR 1
12	+ Y 0	+ PAIR 1
24	- Y 1	- PAIR 2
11	+ Y 1	+ PAIR 2
23	- Y 2	- PAIR 3
10	+ Y 2	+ PAIR 3
22	- Y CLK	- PAIR 4
9	+ Y CLK	+ PAIR 4
21	- Y 3	- PAIR 5
8	+ Y 3	+ PAIR 5
20	100 ohm	+ PAIR 6
7	100 ohm	- PAIR 6
19	- Z 0	- PAIR 7
6	+ Z 0	+ PAIR 7
18	- Z 1	- PAIR 8
5	+ Z 1	+ PAIR 8
17	- Z 2	+ PAIR 9
4	+ Z 2	- PAIR 9
16	- Z CLK	- PAIR 10
3	+ Z CLK	+ PAIR 10
15	- Z 3	+ PAIR 11
2	+ Z 3	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 3b. Pin assignments for the second (Full) 26 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- X 0	- PAIR 1
15	+ X 0	+ PAIR 1
3	- X 1	- PAIR 2
16	+ X 1	+ PAIR 2
4	- X 2	- PAIR 3
17	+ X 2	+ PAIR 3
5	- X CLK	- PAIR 4
18	+ X CLK	+ PAIR 4
6	- X 3	- PAIR 5
19	+ X 3	+ PAIR 5
7	+ SerTC	+ PAIR 6
20	- SerTC	- PAIR 6
8	- SerTFG	- PAIR 7
21	+ SerTFG	+ PAIR 7
9	- CC 1	- PAIR 8
22	+ CC 1	+ PAIR 8
10	+ CC 2	+ PAIR 9
23	- CC 2	- PAIR 9
11	- CC 3	- PAIR 10
24	+ CC 3	+ PAIR 10
12	+ CC 4	+ PAIR 11
25	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 4a. Pin assignments for the first (Base) 26 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- Y 0	- PAIR 1
15	+ Y 0	+ PAIR 1
3	- Y 1	- PAIR 2
16	+ Y 1	+ PAIR 2
4	- Y 2	- PAIR 3
17	+ Y 2	+ PAIR 3
5	- Y CLK	- PAIR 4
18	+ Y CLK	+ PAIR 4
6	- Y 3	- PAIR 5
19	+ Y 3	+ PAIR 5
7	100 ohm	+ PAIR 6
20	100 ohm	- PAIR 6
8	- Z 0	- PAIR 7
21	+ Z 0	+ PAIR 7
9	- Z 1	- PAIR 8
22	+ Z 1	+ PAIR 8
10	- Z 2	+ PAIR 9
23	+ Z 2	- PAIR 9
11	- Z CLK	- PAIR 10
24	+ Z CLK	+ PAIR 10
12	- Z 3	+ PAIR 11
25	+ Z 3	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 4b. Pin assignments for the second (Full) 26 pins output connector.

OPERATING INSTRUCTIONS:

1. Connect AC-DC adaptor to CLCL repeater. Green LED should be on.
2. Connect the Camera Link output(s) of the source to the appropriate CLCL input(s) through a Camera Link cable(s) (not supplied).
3. Connect the CLCL output(s) to the corresponding input(s) of receiving device.
4. Observe the source' Camera Link format (Base, Medium or Full) and connect the corresponding cables to the appropriate input connectors. Medium and Full configuration share the same connector.
5. Power requirements – 6.0 VDC, 300 mA.

Common problems:

1. The unit has no power due to loose DC connector or lack of AC. Check green LED.
2. If the unit generates an output signal but image is corrupted or unstable check the cables and make sure they are firmly attached.

2.3 LVLV – LVDS Repeater

LVLV is an LVDS repeater (30 meter extender), design to extend the distance between any high-resolution digital LVDS camera and any standard LVDS frame grabber by up to 30 meters (100 feet). It reconditions and converts the standard LVDS input interface signals to a standard LVDS output interface – Figure 6. LVLV supports 32 data signals, 4 control signals, 4 enable signals, one data clock signal, and one RS232 serial interface. The maximum data clock is 66 MHz. Figure 7 shows back and front views of the LVLV. Table 5 describes the pin assignments for the 100 pin input connectors. Table 6 describes the pin assignments for the 100 pin output connectors. Detailed views of the LVDS connectors are shown in Appendix 1.

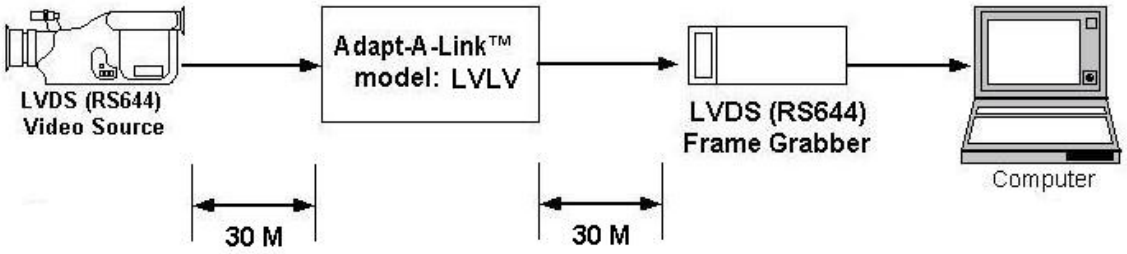

Figure 6. LVLV Connectivity.

Figure 7. LVLV front (top) and back (bottom) views.

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 0	1	51	+ DATA IN 16
- DATA IN 0	2	52	- DATA IN 16
+ DATA IN 1	3	53	+ DATA IN 17
- DATA IN 1	4	54	- DATA IN 17
+ DATA IN 2	5	55	+ DATA IN 18
- DATA IN 2	6	56	- DATA IN 18
+ DATA IN 3	7	57	+ DATA IN 19
- DATA IN 3	8	58	- DATA IN 19
+ DATA IN 4	9	59	+ DATA IN 20
- DATA IN 4	10	60	- DATA IN 20
+ DATA IN 5	11	61	+ DATA IN 21
- DATA IN 5	12	62	- DATA IN 21
+ DATA IN 6	13	63	+ DATA IN 22
- DATA IN 6	14	64	- DATA IN 22
+ DATA IN 7	15	65	+ DATA IN 23
- DATA IN 7	16	66	- DATA IN 23
+ DATA IN 8	17	67	+ DATA IN 24
- DATA IN 8	18	68	- DATA IN 24
+ DATA IN 9	19	69	+ DATA IN 25
- DATA IN 9	20	70	- DATA IN 25
+ DATA IN 10	21	71	+ DATA IN 26
- DATA IN 10	22	72	- DATA IN 26
+ DATA IN 11	23	73	+ DATA IN 27
- DATA IN 11	24	74	- DATA IN 27
+ DATA IN 12	25	75	+ DATA IN 28
- DATA IN 12	26	76	- DATA IN 28
+ DATA IN 13	27	77	+ DATA IN 29
- DATA IN 13	28	78	- DATA IN 29
+ DATA IN 14	29	79	+ DATA IN 30
- DATA IN 14	30	80	- DATA IN 30
+ DATA IN 15	31	81	+ DATA IN 31
- DATA IN 15	32	82	- DATA IN 31
+ CONTROL OUT 0	33	83	N/C
- CONTROL OUT 0	34	84	N/C
+ CONTROL OUT 1	35	85	N/C
- CONTROL OUT 1	36	86	N/C
+ CONTROL OUT 2	37	87	N/C
- CONTROL OUT 2	38	88	N/C
+ CONTROL OUT 3	39	89	N/C
- CONTROL OUT 3	40	90	N/C
+ ENABLE IN 0	41	91	RS232 Rx
- ENABLE IN 0	42	92	RS232 Tx
+ ENABLE IN 1	43	93	SERIAL DATA OUT
- ENABLE IN 1	44	94	SERIAL DATA IN
+ ENABLE IN 2	45	95	+ 6.0 VDC IN
- ENABLE IN 2	46	96	6.0 VDC GROUND
+ ENABLE IN 3	47	97	+ 6.0 VDC IN
- ENABLE IN 3	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN	49	99	GROUND
- PIXEL CLOCK IN	50	100	GROUND

Table 5. Pin assignments for the 100 pins input connector.

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 0	50	100	+ DATA OUT 16
- DATA OUT 0	49	99	- DATA OUT 16
+ DATA OUT 1	48	98	+ DATA OUT 17
- DATA OUT 1	47	97	- DATA OUT 17
+ DATA OUT 2	46	96	+ DATA OUT 18
- DATA OUT 2	45	95	- DATA OUT 18
+ DATA OUT 3	44	94	+ DATA OUT 19
- DATA OUT 3	43	93	- DATA OUT 19
+ DATA OUT 4	42	92	+ DATA OUT 20
- DATA OUT 4	41	91	- DATA OUT 20
+ DATA OUT 5	40	90	+ DATA OUT 21
- DATA OUT 5	39	89	- DATA OUT 21
+ DATA OUT 6	38	88	+ DATA OUT 22
- DATA OUT 6	37	87	- DATA OUT 22
+ DATA OUT 7	36	86	+ DATA OUT 23
- DATA OUT 7	35	85	- DATA OUT 23
+ DATA OUT 8	34	84	N/C
- DATA OUT 8	33	83	N/C
+ DATA OUT 9	32	82	N/C
- DATA OUT 9	31	81	N/C
+ DATA OUT 10	30	80	N/C
- DATA OUT 10	29	79	N/C
+ DATA OUT 11	28	78	N/C
- DATA OUT 11	27	77	N/C
+ DATA OUT 12	26	76	N/C
- DATA OUT 12	25	75	N/C
+ DATA OUT 13	24	74	N/C
- DATA OUT 13	23	73	N/C
+ DATA OUT 14	22	72	N/C
- DATA OUT 14	21	71	N/C
+ DATA OUT 15	20	70	N/C
- DATA OUT 15	19	69	N/C
+ CONTROL IN 0	18	68	N/C
- CONTROL IN 0	17	67	N/C
+ CONTROL IN 1	16	66	N/C
- CONTROL IN 1	15	65	N/C
+ CONTROL IN 2	14	64	N/C
- CONTROL IN 2	13	63	N/C
+ CONTROL IN 3	12	62	N/C
- CONTROL IN 3	11	61	N/C
+ ENABLE OUT 0	10	60	RS232 Tx
- ENABLE OUT 0	9	59	RS232 Rx
+ ENABLE OUT 1	8	58	SERIAL DATA IN
- ENABLE OUT 1	7	57	SERIAL DATA OUT
+ ENABLE OUT 2	6	56	+ 6.0 VDC OUT
- ENABLE OUT 2	5	55	6.0 VDC GROUND
+ ENABLE OUT 3	4	54	+ 6.0 VDC OUT
- ENABLE OUT 3	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT	2	52	GROUND
- PIXEL CLOCK OUT	1	51	GROUND

Table 6. Pin assignments for the 100 pins output connector.

SIGNAL INFORMATION

1. DATA (0 – 31) – 32 bit actual data.
2. ENABLE (0 – 3) – 4 sync signals (usually LVAL, DVAL, FVAL).
3. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.).
4. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
5. SERIAL DATA IN - Serial communications signal going to the camera (Ser TC).
6. SERIAL DATA OUT - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
7. RS232 Rx - Serial communications signal going to the camera (Ser TC).
8. RS232 Tx - Serial communications signal going to the frame grabber (Ser TFG).
9. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
10. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
11. 6.0 VDC GROUND - Provides ground return from the next Adapt-A-Link unit in the chain.

OPERATING INSTRUCTIONS:

1. Connect AC-DC adaptor to LVLV repeater. Green LED should be on.
2. Connect the LVDS output of the source to the LVLV input through an appropriate cable.
3. Connect the LVLV output to the corresponding input of receiving device.
4. Power requirements – 6.0 VDC, 300 mA.

Common problems:

1. The unit has no power due to loose DC connector or lack of AC. Check green LED.
2. If the unit generates an output signal but image is corrupted or unstable check the cables and make sure they are firmly attached.
3. If the unit has power, but there is no output signal, check the cable pin mapping and the polarity of the enable signals.

2.4 BCL – Base Camera Link to LVDS Converter

BCL is designed to interface any high-resolution digital Camera Link camera to any standard LVDS frame grabber. It converts the standard base configuration Camera Link interface signals to a standard LVDS (RS644) output interface – Figure 8. BCL supports 24 data signals, 4 control signals, 4 enable signals, one clock signal, and one RS232 serial interface. The maximum data clock is 66 MHz. Figure 9 shows back and front views of the BCL. Table 7 describes the bit assignments for base Camera Link interface. Table 8 describes the pin assignments for the 100 pin output connector. Table 9 describes the pin assignments for the 26 pin Camera Link input connector. Detailed views of the Camera link input and LVDS output connectors are shown in Appendix 1.

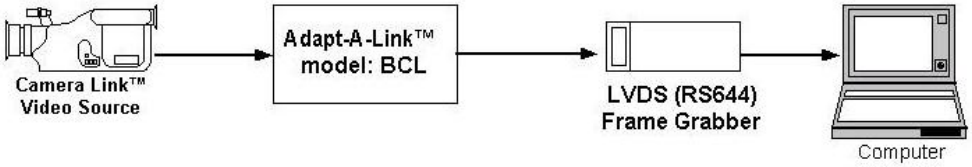

Figure 8. BCL Connectivity.

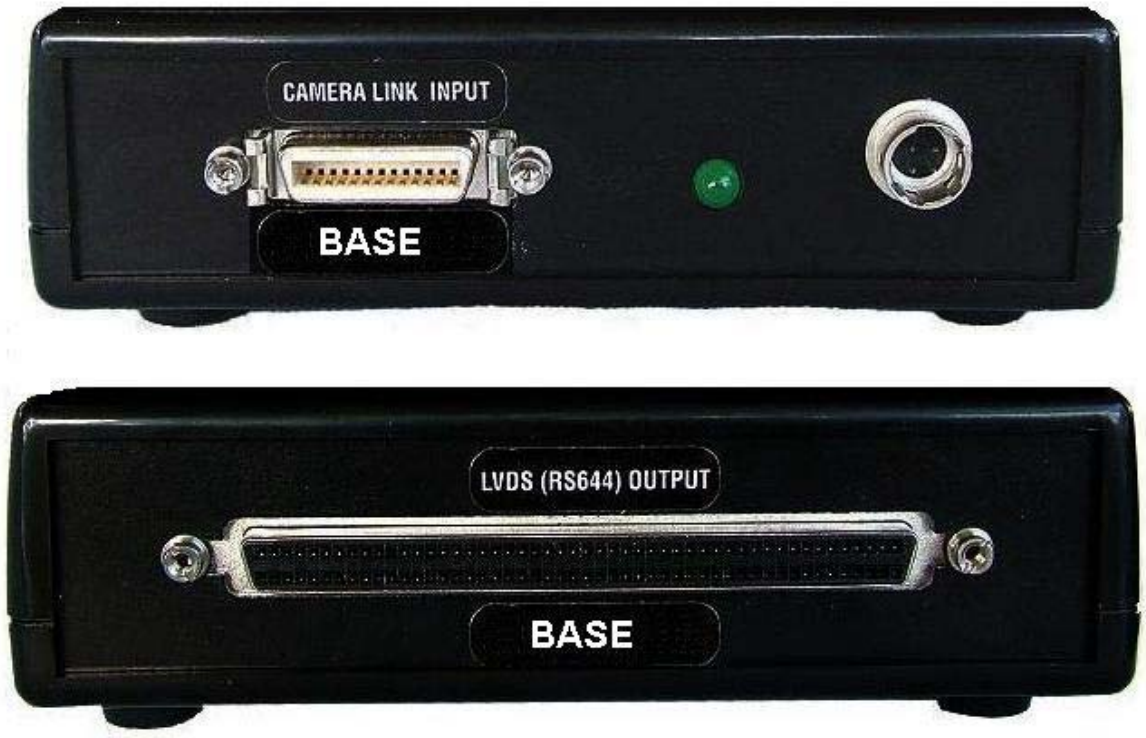

Figure 9. BCL front (top) and back (bottom) views.

DATA	Port/bit	1/3 Taps 8-bits	1/2 Taps 10-bits	1/2 Taps 12-bits	1 Tap 14-bits	1 Tap 16-bits	24-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0
DATA 9	Port B1	B1	A9	A9	A9	A9	G1
DATA 10	Port B2	B2	nc	A10	A10	A10	G2
DATA 11	Port B3	B3	nc	A11	A11	A11	G3
DATA 12	Port B4	B4	B8	B8	A12	A12	G4
DATA 13	Port B5	B5	B9	B9	A13	A13	G5
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 7. Bit assignments for base Camera Link interface.

SIGNAL INFORMATION

1. ENABLE (0 – 3) – 4 sync signals (usually LVAL, DVAL, FVAL).
2. LVAL - Line Valid is defined HIGH (default) for valid pixels.
3. DVAL - Data Valid is defined HIGH (default) when the data is valid.
4. FVAL - Frame Valid is defined HIGH (default) for valid lines.
5. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
6. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.).

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 0	50	100	+ DATA OUT 16
- DATA OUT 0	49	99	- DATA OUT 16
+ DATA OUT 1	48	98	+ DATA OUT 17
- DATA OUT 1	47	97	- DATA OUT 17
+ DATA OUT 2	46	96	+ DATA OUT 18
- DATA OUT 2	45	95	- DATA OUT 18
+ DATA OUT 3	44	94	+ DATA OUT 19
- DATA OUT 3	43	93	- DATA OUT 19
+ DATA OUT 4	42	92	+ DATA OUT 20
- DATA OUT 4	41	91	- DATA OUT 20
+ DATA OUT 5	40	90	+ DATA OUT 21
- DATA OUT 5	39	89	- DATA OUT 21
+ DATA OUT 6	38	88	+ DATA OUT 22
- DATA OUT 6	37	87	- DATA OUT 22
+ DATA OUT 7	36	86	+ DATA OUT 23
- DATA OUT 7	35	85	- DATA OUT 23
+ DATA OUT 8	34	84	N/C
- DATA OUT 8	33	83	N/C
+ DATA OUT 9	32	82	N/C
- DATA OUT 9	31	81	N/C
+ DATA OUT 10	30	80	N/C
- DATA OUT 10	29	79	N/C
+ DATA OUT 11	28	78	N/C
- DATA OUT 11	27	77	N/C
+ DATA OUT 12	26	76	N/C
- DATA OUT 12	25	75	N/C
+ DATA OUT 13	24	74	N/C
- DATA OUT 13	23	73	N/C
+ DATA OUT 14	22	72	N/C
- DATA OUT 14	21	71	N/C
+ DATA OUT 15	20	70	N/C
- DATA OUT 15	19	69	N/C
+ CONTROL IN 0	18	68	N/C
- CONTROL IN 0	17	67	N/C
+ CONTROL IN 1	16	66	N/C
- CONTROL IN 1	15	65	N/C
+ CONTROL IN 2	14	64	N/C
- CONTROL IN 2	13	63	N/C
+ CONTROL IN 3	12	62	N/C
- CONTROL IN 3	11	61	N/C
+ ENABLE OUT 0	10	60	RS232 Tx
- ENABLE OUT 0	9	59	RS232 Rx
+ ENABLE OUT 1	8	58	SERIAL DATA IN
- ENABLE OUT 1	7	57	SERIAL DATA OUT
+ ENABLE OUT 2	6	56	+ 6.0 VDC OUT
- ENABLE OUT 2	5	55	6.0 VDC GROUND
+ ENABLE OUT 3	4	54	+ 6.0 VDC OUT
- ENABLE OUT 3	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT	2	52	GROUND
- PIXEL CLOCK OUT	1	51	GROUND

Table 8. Pin assignments for the 100 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- X 0	- PAIR 1
12	+ X 0	+ PAIR 1
24	- X 1	- PAIR 2
11	+ X 1	+ PAIR 2
23	- X 2	- PAIR 3
10	+ X 2	+ PAIR 3
22	- X CLK	- PAIR 4
9	+ X CLK	+ PAIR 4
21	- X 3	- PAIR 5
8	+ X 3	+ PAIR 5
20	+ SerTC	+ PAIR 6
7	- SerTC	- PAIR 6
19	- SerTFG	- PAIR 7
6	+ SerTFG	+ PAIR 7
18	- CC 1	- PAIR 8
5	+ CC 1	+ PAIR 8
17	+ CC 2	+ PAIR 9
4	- CC 2	- PAIR 9
16	- CC 3	- PAIR 10
3	+ CC 3	+ PAIR 10
15	+ CC 4	+ PAIR 11
2	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 9. Pin assignments for the 26 pins input connector.

SIGNAL INFORMATION

1. DATA (0 – 23) – 24 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
3. SERIAL DATA IN - Serial communications signal going to the camera (Ser TC).
4. SERIAL DATA OUT - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
5. RS232 Rx - Serial communications signal going to the camera (Ser TC)
6. RS232 Tx - Serial communications signal going to the frame grabber (Ser TFG).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected.

2.5 BCR – Base Camera Link to RS422 Converter

BCR is designed to interface any high-resolution digital Camera Link camera to any standard RS422 frame grabber. It converts the standard base configuration Camera Link interface signals to a standard RS422 output interface – Figure 10. BCR supports 24 data signals, 4 control signals, 4 enable signals, one clock signal, and one RS232 serial interface. The maximum data clock is 33 MHz. Figure 11 shows back and front views of the BCR. Table 10 describes the bit assignments for base Camera Link interface. Table 11 describes the pin assignments for the 100 pin output connector. Table 12 describes the pin assignments for the 26 pin Camera Link input connector. Detailed views of the Camera link input and RS422 output connectors are shown in Appendix 1.

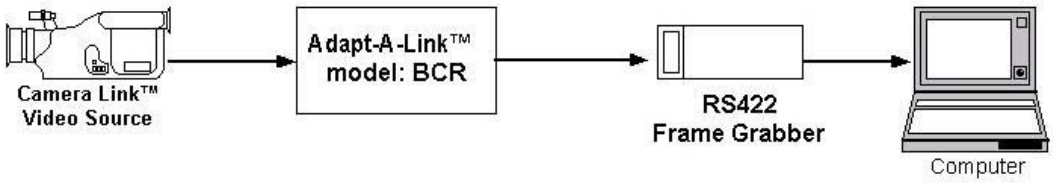

Figure 10. BCR Connectivity.

Figure 11. BCR front (top) and back (bottom) views.

DATA	Port/bit	1/3 Taps 8-bits	1/2 Taps 10-bits	1/2 Taps 12-bits	1 Tap 14-bits	1 Tap 16-bits	24-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0
DATA 9	Port B1	B1	A9	A9	A9	A9	G1
DATA 10	Port B2	B2	nc	A10	A10	A10	G2
DATA 11	Port B3	B3	nc	A11	A11	A11	G3
DATA 12	Port B4	B4	B8	B8	A12	A12	G4
DATA 13	Port B5	B5	B9	B9	A13	A13	G5
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 10. Bit assignments for base Camera Link interface.

SIGNAL INFORMATION

1. ENABLE (0 – 3) – 4 sync signals (usually LVAL, DVAL, FVAL)
2. LVAL - Line Valid is defined HIGH (default) for valid pixels.
3. DVAL - Data Valid is defined HIGH (default) when the data is valid.
4. FVAL - Frame Valid is defined HIGH (default) for valid lines.
5. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
6. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.)

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 0	50	100	+ DATA OUT 16
- DATA OUT 0	49	99	- DATA OUT 16
+ DATA OUT 1	48	98	+ DATA OUT 17
- DATA OUT 1	47	97	- DATA OUT 17
+ DATA OUT 2	46	96	+ DATA OUT 18
- DATA OUT 2	45	95	- DATA OUT 18
+ DATA OUT 3	44	94	+ DATA OUT 19
- DATA OUT 3	43	93	- DATA OUT 19
+ DATA OUT 4	42	92	+ DATA OUT 20
- DATA OUT 4	41	91	- DATA OUT 20
+ DATA OUT 5	40	90	+ DATA OUT 21
- DATA OUT 5	39	89	- DATA OUT 21
+ DATA OUT 6	38	88	+ DATA OUT 22
- DATA OUT 6	37	87	- DATA OUT 22
+ DATA OUT 7	36	86	+ DATA OUT 23
- DATA OUT 7	35	85	- DATA OUT 23
+ DATA OUT 8	34	84	N/C
- DATA OUT 8	33	83	N/C
+ DATA OUT 9	32	82	N/C
- DATA OUT 9	31	81	N/C
+ DATA OUT 10	30	80	N/C
- DATA OUT 10	29	79	N/C
+ DATA OUT 11	28	78	N/C
- DATA OUT 11	27	77	N/C
+ DATA OUT 12	26	76	N/C
- DATA OUT 12	25	75	N/C
+ DATA OUT 13	24	74	N/C
- DATA OUT 13	23	73	N/C
+ DATA OUT 14	22	72	N/C
- DATA OUT 14	21	71	N/C
+ DATA OUT 15	20	70	N/C
- DATA OUT 15	19	69	N/C
+ CONTROL IN 0	18	68	N/C
- CONTROL IN 0	17	67	N/C
+ CONTROL IN 1	16	66	N/C
- CONTROL IN 1	15	65	N/C
+ CONTROL IN 2	14	64	N/C
- CONTROL IN 2	13	63	N/C
+ CONTROL IN 3	12	62	N/C
- CONTROL IN 3	11	61	N/C
+ ENABLE OUT 0	10	60	RS232 Tx
- ENABLE OUT 0	9	59	RS232 Rx
+ ENABLE OUT 1	8	58	SERIAL DATA IN
- ENABLE OUT 1	7	57	SERIAL DATA OUT
+ ENABLE OUT 2	6	56	+ 6.0 VDC OUT
- ENABLE OUT 2	5	55	6.0 VDC GROUND
+ ENABLE OUT 3	4	54	+ 6.0 VDC OUT
- ENABLE OUT 3	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT	2	52	GROUND
- PIXEL CLOCK OUT	1	51	GROUND

Table 11. Pin assignments for the 100 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- X 0	- PAIR 1
12	+ X 0	+ PAIR 1
24	- X 1	- PAIR 2
11	+ X 1	+ PAIR 2
23	- X 2	- PAIR 3
10	+ X 2	+ PAIR 3
22	- X CLK	- PAIR 4
9	+ X CLK	+ PAIR 4
21	- X 3	- PAIR 5
8	+ X 3	+ PAIR 5
20	+ SerTC	+ PAIR 6
7	- SerTC	- PAIR 6
19	- SerTFG	- PAIR 7
6	+ SerTFG	+ PAIR 7
18	- CC 1	- PAIR 8
5	+ CC 1	+ PAIR 8
17	+ CC 2	+ PAIR 9
4	- CC 2	- PAIR 9
16	- CC 3	- PAIR 10
3	+ CC 3	+ PAIR 10
15	+ CC 4	+ PAIR 11
2	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 12. Pin assignments for the 26 pins input connector.

SIGNAL INFORMATION

1. DATA (0 – 23) – 24 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 33 MHz.
3. SERIAL DATA IN - Serial communications signal going to the camera (Ser TC).
4. SERIAL DATA OUT - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
5. RS232 Rx - Serial communications signal going to the camera (Ser TC)
6. RS232 Tx - Serial communications signal going to the frame grabber (Ser TFG).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected.

2.6 BLC – LVDS to Base Camera Link Converter

BLC is designed to interface any high-resolution digital LVDS camera to any standard Camera Link frame grabber. It converts the standard LVDS (RS644) interface signals to a standard base configuration Camera Link output interface – Figure 12. BLC supports 24 data signals, 4 control signals, 4 enable signals, one clock signal, and one RS232 serial interface. The maximum data clock is 66 MHz. Figure 13 shows back and front view of the BLC. Table 13 describes the bit assignments for base Camera Link interface. Table 14 describes the pin assignments for the 100 pin input connector. Table 15 describes the pin assignments for the 26 pin Camera Link output connector. Detailed views of the LVDS input and Camera link output connectors are shown in Appendix 1.

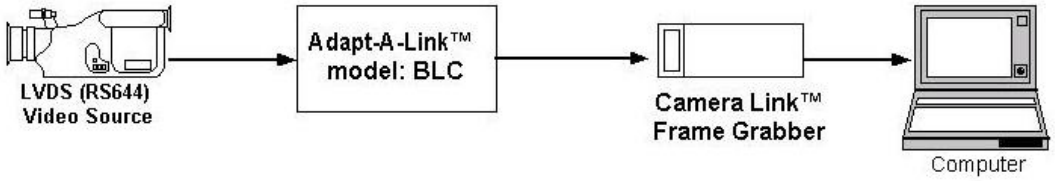

Figure 12. BLC Connectivity.

Figure 13. BLC front (top) and back (bottom) views.

DATA	Port/bit	1/3 Taps 8-bits	1/2 Taps 10-bits	1/2 Taps 12-bits	1 Tap 14-bits	1 Tap 16-bits	24-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0
DATA 9	Port B1	B1	A9	A9	A9	A9	G1
DATA 10	Port B2	B2	nc	A10	A10	A10	G2
DATA 11	Port B3	B3	nc	A11	A11	A11	G3
DATA 12	Port B4	B4	B8	B8	A12	A12	G4
DATA 13	Port B5	B5	B9	B9	A13	A13	G5
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 13. Bit assignments for base Camera Link interface.

SIGNAL INFORMATION

1. ENABLE (0 – 3) – 4 sync signals (usually LVAL, DVAL, FVAL)
2. LVAL - Line Valid is defined HIGH (default) for valid pixels.
3. DVAL - Data Valid is defined HIGH (default) when the data is valid.
4. FVAL - Frame Valid is defined HIGH (default) for valid lines.
5. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
6. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.)

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 0	1	51	+ DATA IN 16
- DATA IN 0	2	52	- DATA IN 16
+ DATA IN 1	3	53	+ DATA IN 17
- DATA IN 1	4	54	- DATA IN 17
+ DATA IN 2	5	55	+ DATA IN 18
- DATA IN 2	6	56	- DATA IN 18
+ DATA IN 3	7	57	+ DATA IN 19
- DATA IN 3	8	58	- DATA IN 19
+ DATA IN 4	9	59	+ DATA IN 20
- DATA IN 4	10	60	- DATA IN 20
+ DATA IN 5	11	61	+ DATA IN 21
- DATA IN 5	12	62	- DATA IN 21
+ DATA IN 6	13	63	+ DATA IN 22
- DATA IN 6	14	64	- DATA IN 22
+ DATA IN 7	15	65	+ DATA IN 23
- DATA IN 7	16	66	- DATA IN 23
+ DATA IN 8	17	67	N/C
- DATA IN 8	18	68	N/C
+ DATA IN 9	19	69	N/C
- DATA IN 9	20	70	N/C
+ DATA IN 10	21	71	N/C
- DATA IN 10	22	72	N/C
+ DATA IN 11	23	73	N/C
- DATA IN 11	24	74	N/C
+ DATA IN 12	25	75	N/C
- DATA IN 12	26	76	N/C
+ DATA IN 13	27	77	N/C
- DATA IN 13	28	78	N/C
+ DATA IN 14	29	79	N/C
- DATA IN 14	30	80	N/C
+ DATA IN 15	31	81	N/C
- DATA IN 15	32	82	N/C
+ CONTROL OUT 0	33	83	N/C
- CONTROL OUT 0	34	84	N/C
+ CONTROL OUT 1	35	85	N/C
- CONTROL OUT 1	36	86	N/C
+ CONTROL OUT 2	37	87	N/C
- CONTROL OUT 2	38	88	N/C
+ CONTROL OUT 3	39	89	N/C
- CONTROL OUT 3	40	90	N/C
+ ENABLE IN 0	41	91	RS232 Rx
- ENABLE IN 0	42	92	RS232 Tx
+ ENABLE IN 1	43	93	SERIAL DATA OUT
- ENABLE IN 1	44	94	SERIAL DATA IN
+ ENABLE IN 2	45	95	+ 6.0 VDC IN
- ENABLE IN 2	46	96	6.0 VDC GROUND
+ ENABLE IN 3	47	97	+ 6.0 VDC IN
- ENABLE IN 3	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN	49	99	GROUND
- PIXEL CLOCK IN	50	100	GROUND

Table 14. Pin assignments for the 100 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- X 0	- PAIR 1
15	+ X 0	+ PAIR 1
3	- X 1	- PAIR 2
16	+ X 1	+ PAIR 2
4	- X 2	- PAIR 3
17	+ X 2	+ PAIR 3
5	- X CLK	- PAIR 4
18	+ X CLK	+ PAIR 4
6	- X 3	- PAIR 5
19	+ X 3	+ PAIR 5
7	+ SerTC	+ PAIR 6
20	- SerTC	- PAIR 6
8	- SerTFG	- PAIR 7
21	+ SerTFG	+ PAIR 7
9	- CC 1	- PAIR 8
22	+ CC 1	+ PAIR 8
10	+ CC 2	+ PAIR 9
23	- CC 2	- PAIR 9
11	- CC 3	- PAIR 10
24	+ CC 3	+ PAIR 10
12	+ CC 4	+ PAIR 11
25	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 15. Pin assignments for the 26 pins output connector.

SIGNAL INFORMATION

1. DATA (0 – 23) – 24 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
3. SERIAL DATA IN - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
4. SERIAL DATA OUT - Serial communications signal going to the camera (Ser TC).
5. RS232 Rx - Serial communications signal going to the frame grabber (Ser TFG)
6. RS232 Tx - Serial communications signal going to the camera (Ser TC).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected.

2.7 BRC – RS422 to Base Camera Link Converter

BRC is designed to interface any high-resolution digital RS422 camera to any standard Camera Link frame grabber. It converts the standard RS422 interface signals to a standard base configuration Camera Link output interface – Figure 14. BRC supports 24 data signals, 4 control signals, 4 enable signals, one clock signal, and one RS232 serial interface. The maximum data clock is 33 MHz. Figure 15 shows back and front views of the BRC. Table 16 describes the bit assignments for base Camera Link interface. Table 17 describes the pin assignments for the 100 pin input connector. Table 18 describes the pin assignments for the 26 pin Camera Link output connector. Detailed views of the RS422 input and Camera link output connectors are shown in Appendix 1.

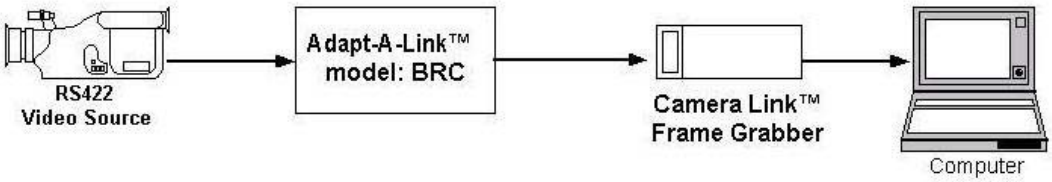

Figure 14. BRC Connectivity.

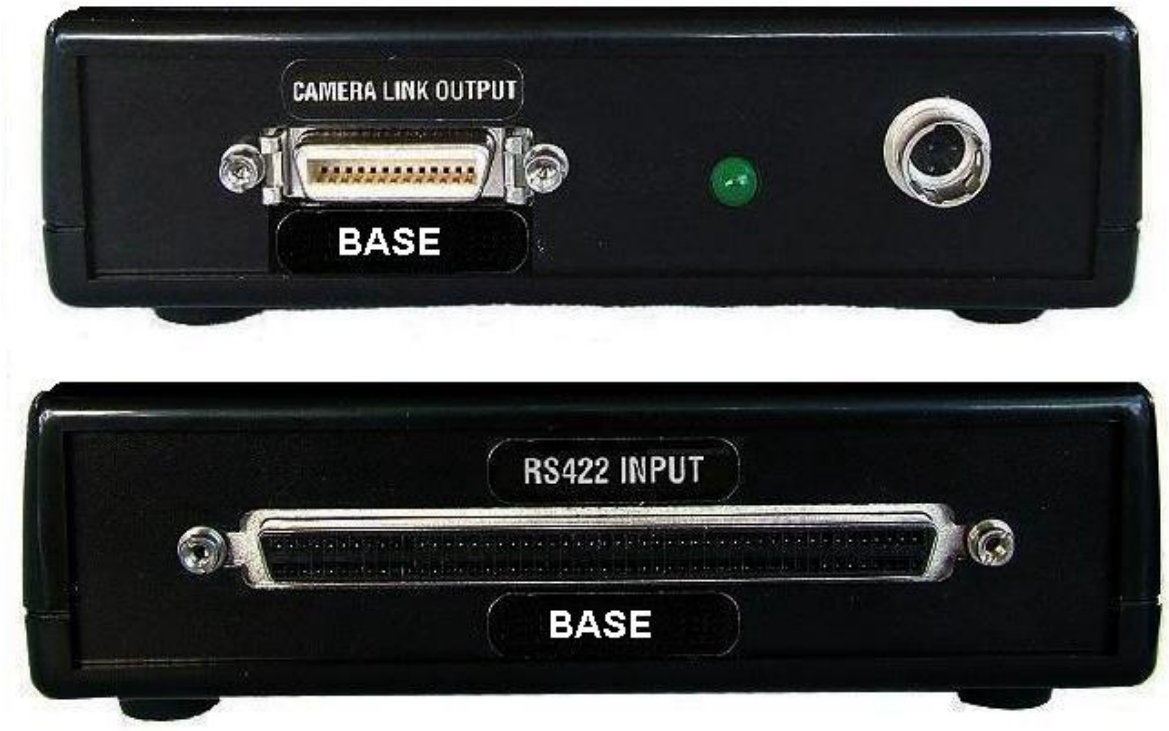

Figure 15. BRC front (top) and back (bottom) views.

DATA	Port/bit	1/3 Taps 8-bits	1/2 Taps 10-bits	1/2 Taps 12-bits	1 Tap 14-bits	1 Tap 16-bits	24-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0
DATA 9	Port B1	B1	A9	A9	A9	A9	G1
DATA 10	Port B2	B2	nc	A10	A10	A10	G2
DATA 11	Port B3	B3	nc	A11	A11	A11	G3
DATA 12	Port B4	B4	B8	B8	A12	A12	G4
DATA 13	Port B5	B5	B9	B9	A13	A13	G5
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 16. Bit assignments for base Camera Link interface.

SIGNAL INFORMATION

1. ENABLE (0 – 3) – 4 sync signals (usually LVAL, DVAL, FVAL)
2. LVAL - Line Valid is defined HIGH (default) for valid pixels.
3. DVAL - Data Valid is defined HIGH (default) when the data is valid.
4. FVAL - Frame Valid is defined HIGH (default) for valid lines.
5. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
6. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.)

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 0	1	51	+ DATA IN 16
- DATA IN 0	2	52	- DATA IN 16
+ DATA IN 1	3	53	+ DATA IN 17
- DATA IN 1	4	54	- DATA IN 17
+ DATA IN 2	5	55	+ DATA IN 18
- DATA IN 2	6	56	- DATA IN 18
+ DATA IN 3	7	57	+ DATA IN 19
- DATA IN 3	8	58	- DATA IN 19
+ DATA IN 4	9	59	+ DATA IN 20
- DATA IN 4	10	60	- DATA IN 20
+ DATA IN 5	11	61	+ DATA IN 21
- DATA IN 5	12	62	- DATA IN 21
+ DATA IN 6	13	63	+ DATA IN 22
- DATA IN 6	14	64	- DATA IN 22
+ DATA IN 7	15	65	+ DATA IN 23
- DATA IN 7	16	66	- DATA IN 23
+ DATA IN 8	17	67	N/C
- DATA IN 8	18	68	N/C
+ DATA IN 9	19	69	N/C
- DATA IN 9	20	70	N/C
+ DATA IN 10	21	71	N/C
- DATA IN 10	22	72	N/C
+ DATA IN 11	23	73	N/C
- DATA IN 11	24	74	N/C
+ DATA IN 12	25	75	N/C
- DATA IN 12	26	76	N/C
+ DATA IN 13	27	77	N/C
- DATA IN 13	28	78	N/C
+ DATA IN 14	29	79	N/C
- DATA IN 14	30	80	N/C
+ DATA IN 15	31	81	N/C
- DATA IN 15	32	82	N/C
+ CONTROL OUT 0	33	83	N/C
- CONTROL OUT 0	34	84	N/C
+ CONTROL OUT 1	35	85	N/C
- CONTROL OUT 1	36	86	N/C
+ CONTROL OUT 2	37	87	N/C
- CONTROL OUT 2	38	88	N/C
+ CONTROL OUT 3	39	89	N/C
- CONTROL OUT 3	40	90	N/C
+ ENABLE IN 0	41	91	RS232 Rx
- ENABLE IN 0	42	92	RS232 Tx
+ ENABLE IN 1	43	93	SERIAL DATA OUT
- ENABLE IN 1	44	94	SERIAL DATA IN
+ ENABLE IN 2	45	95	+ 6.0 VDC IN
- ENABLE IN 2	46	96	6.0 VDC GROUND
+ ENABLE IN 3	47	97	+ 6.0 VDC IN
- ENABLE IN 3	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN	49	99	GROUND
- PIXEL CLOCK IN	50	100	GROUND

Table 17. Pin assignments for the 100 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- X 0	- PAIR 1
15	+ X 0	+ PAIR 1
3	- X 1	- PAIR 2
16	+ X 1	+ PAIR 2
4	- X 2	- PAIR 3
17	+ X 2	+ PAIR 3
5	- X CLK	- PAIR 4
18	+ X CLK	+ PAIR 4
6	- X 3	- PAIR 5
19	+ X 3	+ PAIR 5
7	+ SerTC	+ PAIR 6
20	- SerTC	- PAIR 6
8	- SerTFG	- PAIR 7
21	+ SerTFG	+ PAIR 7
9	- CC 1	- PAIR 8
22	+ CC 1	+ PAIR 8
10	+ CC 2	+ PAIR 9
23	- CC 2	- PAIR 9
11	- CC 3	- PAIR 10
24	+ CC 3	+ PAIR 10
12	+ CC 4	+ PAIR 11
25	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 18. Pin assignments for the 26 pins output connector.

SIGNAL INFORMATION

1. DATA (0 – 23) – 24 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 33 MHz.
3. SERIAL DATA IN - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
4. SERIAL DATA OUT - Serial communications signal going to the camera (Ser TC).
5. RS232 Rx - Serial communications signal going to the frame grabber (Ser TFG)
6. RS232 Tx - Serial communications signal going to the camera (Ser TC).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected.

2.8 MCL – Medium Camera Link to LVDS Converter

MCL is designed to interface any high-resolution digital Camera Link camera to any standard LVDS frame grabber. It converts the standard Medium configuration Camera Link interface signals to a standard LVDS (RS644) output interface – Figure 16. MCL supports 48 data signals, 4 control signals, 8 enable signals, 2 clock signals, and one RS232 serial interface. The maximum data clock is 66 MHz. Figure 17 shows back and front views of the MCL. Table 19 describes the bit assignments for Medium Camera Link interface. Table 20 (a, b) describes the pin assignments for the 100 pin output connectors. Table 21 (a, b) describes the pin assignments for the 26 pin Camera Link input connectors. Detailed views of the Camera link input and LVDS output connectors are shown in Appendix 1.

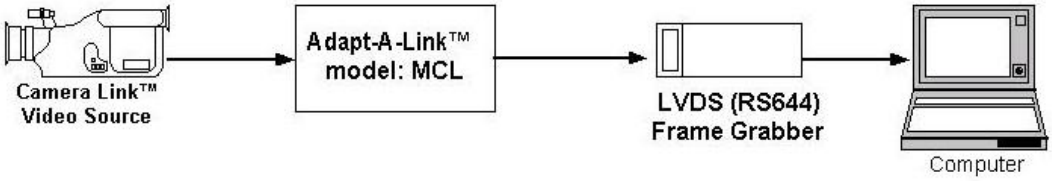

Figure 16. MCL Connectivity.

Figure 17. MCL front (top) and back (bottoms) views.

DATA	Port/bit	1/4 Taps 8-bits	1/4 Taps 10-bits	1/4 Taps 12-bits	1/2 Taps 14-bits	1/2 Taps 16-bits	24-bit RGB	30-bit RGB	36-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0	R0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1	R1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2	R2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3	R3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4	R4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5	R5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6	R6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7	R7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0	R8	R8
DATA 9	Port B1	B1	A9	A9	A9	A9	G1	R9	R9
DATA 10	Port B2	B2	nc	A10	A10	A10	G2	N/C	R10
DATA 11	Port B3	B3	nc	A11	A11	A11	G3	N/C	R11
DATA 12	Port B4	B4	B8	B8	A12	A12	G4	B8	B8
DATA 13	Port B5	B5	B9	B9	A13	A13	G5	B9	B9
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6	N/C	B10
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7	N/C	B11
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0	B0	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1	B1	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2	B2	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3	B3	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4	B4	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5	B5	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6	B6	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7	B7	B7
DATA 24	Port D0	D0	D0	D0	B0	B0	N/C	N/C	N/C
DATA 25	Port D1	D1	D1	D1	B1	B1	N/C	N/C	N/C
DATA 26	Port D2	D2	D2	D2	B2	B2	N/C	N/C	N/C
DATA 27	Port D3	D3	D3	D3	B3	B3	N/C	N/C	N/C
DATA 28	Port D4	D4	D4	D4	B4	B4	N/C	N/C	N/C
DATA 29	Port D5	D5	D5	D5	B5	B5	N/C	N/C	N/C
DATA 30	Port D6	D6	D6	D6	B6	B6	N/C	N/C	N/C
DATA 31	Port D7	D7	D7	D7	B7	B7	N/C	N/C	N/C
DATA 32	Port E0	N/C	C0	C0	B8	B8	N/C	G0	G0
DATA 33	Port E1	N/C	C1	C1	B9	B9	N/C	G1	G1
DATA 34	Port E2	N/C	C2	C2	B10	B10	N/C	G2	G2
DATA 35	Port E3	N/C	C3	C3	B11	B11	N/C	G3	G3
DATA 36	Port E4	N/C	C4	C4	B12	B12	N/C	G4	G4
DATA 37	Port E5	N/C	C5	C5	B13	B13	N/C	G5	G5
DATA 38	Port E6	N/C	C6	C6	N/C	B14	N/C	G6	G6
DATA 39	Port E7	N/C	C7	C7	N/C	B15	N/C	G7	G7

DATA 40	Port F0	N/C	C8	C8	N/C	N/C	N/C	G8	G8
DATA 41	Port F1	N/C	C9	C9	N/C	N/C	N/C	G9	G9
DATA 42	Port F2	N/C	N/C	C10	N/C	N/C	N/C	N/C	G10
DATA 43	Port F3	N/C	N/C	C11	N/C	N/C	N/C	N/C	G11
DATA 44	Port F4	N/C	D8	D8	N/C	N/C	N/C	N/C	N/C
DATA 45	Port F5	N/C	D9	D9	N/C	N/C	N/C	N/C	N/C
DATA 46	Port F6	N/C	N/C	D10	N/C	N/C	N/C	N/C	N/C
DATA 47	Port F7	N/C	N/C	D11	N/C	N/C	N/C	N/C	N/C
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
ENABLE 4	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1
ENABLE 5	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1
ENABLE 6	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1
ENABLE 7	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 19. Bit assignments for Medium Camera Link interface.

SIGNAL INFORMATION

1. ENABLE (0 – 7) – 8 sync signals (usually LVAL, DVAL, FVAL).
2. LVAL - Line Valid is defined HIGH (default) for valid pixels.
3. DVAL - Data Valid is defined HIGH (default) when the data is valid.
4. FVAL - Frame Valid is defined HIGH (default) for valid lines.
5. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
6. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.).

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 0	50	100	+ DATA OUT 16
- DATA OUT 0	49	99	- DATA OUT 16
+ DATA OUT 1	48	98	+ DATA OUT 17
- DATA OUT 1	47	97	- DATA OUT 17
+ DATA OUT 2	46	96	+ DATA OUT 18
- DATA OUT 2	45	95	- DATA OUT 18
+ DATA OUT 3	44	94	+ DATA OUT 19
- DATA OUT 3	43	93	- DATA OUT 19
+ DATA OUT 4	42	92	+ DATA OUT 20
- DATA OUT 4	41	91	- DATA OUT 20
+ DATA OUT 5	40	90	+ DATA OUT 21
- DATA OUT 5	39	89	- DATA OUT 21
+ DATA OUT 6	38	88	+ DATA OUT 22
- DATA OUT 6	37	87	- DATA OUT 22
+ DATA OUT 7	36	86	+ DATA OUT 23
- DATA OUT 7	35	85	- DATA OUT 23
+ DATA OUT 8	34	84	N/C
- DATA OUT 8	33	83	N/C
+ DATA OUT 9	32	82	N/C
- DATA OUT 9	31	81	N/C
+ DATA OUT 10	30	80	N/C
- DATA OUT 10	29	79	N/C
+ DATA OUT 11	28	78	N/C
- DATA OUT 11	27	77	N/C
+ DATA OUT 12	26	76	N/C
- DATA OUT 12	25	75	N/C
+ DATA OUT 13	24	74	N/C
- DATA OUT 13	23	73	N/C
+ DATA OUT 14	22	72	N/C
- DATA OUT 14	21	71	N/C
+ DATA OUT 15	20	70	N/C
- DATA OUT 15	19	69	N/C
+ CONTROL IN 0	18	68	N/C
- CONTROL IN 0	17	67	N/C
+ CONTROL IN 1	16	66	N/C
- CONTROL IN 1	15	65	N/C
+ CONTROL IN 2	14	64	N/C
- CONTROL IN 2	13	63	N/C
+ CONTROL IN 3	12	62	N/C
- CONTROL IN 3	11	61	N/C
+ ENABLE OUT 0	10	60	RS232 Tx
- ENABLE OUT 0	9	59	RS232 Rx
+ ENABLE OUT 1	8	58	SERIAL DATA IN
- ENABLE OUT 1	7	57	SERIAL DATA OUT
+ ENABLE OUT 2	6	56	+ 6.0 VDC OUT
- ENABLE OUT 2	5	55	6.0 VDC GROUND
+ ENABLE OUT 3	4	54	+ 6.0 VDC OUT
- ENABLE OUT 3	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT	2	52	GROUND
- PIXEL CLOCK OUT	1	51	GROUND

Table 20a. Pin assignments for the first 100 pins output connector.

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 24	50	100	+ DATA OUT 40
- DATA OUT 24	49	99	- DATA OUT 40
+ DATA OUT 25	48	98	+ DATA OUT 41
- DATA OUT 25	47	97	- DATA OUT 41
+ DATA OUT 26	46	96	+ DATA OUT 42
- DATA OUT 26	45	95	- DATA OUT 42
+ DATA OUT 27	44	94	+ DATA OUT 43
- DATA OUT 27	43	93	- DATA OUT 43
+ DATA OUT 28	42	92	+ DATA OUT 44
- DATA OUT 28	41	91	- DATA OUT 44
+ DATA OUT 29	40	90	+ DATA OUT 45
- DATA OUT 29	39	89	- DATA OUT 45
+ DATA OUT 30	38	88	+ DATA OUT 46
- DATA OUT 30	37	87	- DATA OUT 46
+ DATA OUT 31	36	86	+ DATA OUT 47
- DATA OUT 31	35	85	- DATA OUT 47
+ DATA OUT 32	34	84	N/C
- DATA OUT 32	33	83	N/C
+ DATA OUT 33	32	82	N/C
- DATA OUT 33	31	81	N/C
+ DATA OUT 34	30	80	N/C
- DATA OUT 34	29	79	N/C
+ DATA OUT 35	28	78	N/C
- DATA OUT 35	27	77	N/C
+ DATA OUT 36	26	76	N/C
- DATA OUT 36	25	75	N/C
+ DATA OUT 37	24	74	N/C
- DATA OUT 37	23	73	N/C
+ DATA OUT 38	22	72	N/C
- DATA OUT 38	21	71	N/C
+ DATA OUT 39	20	70	N/C
- DATA OUT 39	19	69	N/C
N/C	18	68	N/C
N/C	17	67	N/C
N/C	16	66	N/C
N/C	15	65	N/C
N/C	14	64	N/C
N/C	13	63	N/C
N/C	12	62	N/C
N/C	11	61	N/C
+ ENABLE OUT 4	10	60	N/C
- ENABLE OUT 4	9	59	N/C
+ ENABLE OUT 5	8	58	N/C
- ENABLE OUT 5	7	57	N/C
+ ENABLE OUT 6	6	56	+ 6.0 VDC OUT
- ENABLE OUT 6	5	55	6.0 VDC GROUND
+ ENABLE OUT 7	4	54	+ 6.0 VDC OUT
- ENABLE OUT 7	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT 1	2	52	GROUND
- PIXEL CLOCK OUT 1	1	51	GROUND

Table 20b. Pin assignments for the second 100 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- X 0	- PAIR 1
12	+ X 0	+ PAIR 1
24	- X 1	- PAIR 2
11	+ X 1	+ PAIR 2
23	- X 2	- PAIR 3
10	+ X 2	+ PAIR 3
22	- X CLK	- PAIR 4
9	+ X CLK	+ PAIR 4
21	- X 3	- PAIR 5
8	+ X 3	+ PAIR 5
20	+ SerTC	+ PAIR 6
7	- SerTC	- PAIR 6
19	- SerTFG	- PAIR 7
6	+ SerTFG	+ PAIR 7
18	- CC 1	- PAIR 8
5	+ CC 1	+ PAIR 8
17	+ CC 2	+ PAIR 9
4	- CC 2	- PAIR 9
16	- CC 3	- PAIR 10
3	+ CC 3	+ PAIR 10
15	+ CC 4	+ PAIR 11
2	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 21a. Pin assignments for the first (Base) 26 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- Y 0	- PAIR 1
12	+ Y 0	+ PAIR 1
24	- Y 1	- PAIR 2
11	+ Y 1	+ PAIR 2
23	- Y 2	- PAIR 3
10	+ Y 2	+ PAIR 3
22	- Y CLK	- PAIR 4
9	+ Y CLK	+ PAIR 4
21	- Y 3	- PAIR 5
8	+ Y 3	+ PAIR 5
20	N/C	+ PAIR 6
7	N/C	- PAIR 6
19	N/C	- PAIR 7
6	N/C	+ PAIR 7
18	N/C	- PAIR 8
5	N/C	+ PAIR 8
17	N/C	+ PAIR 9
4	N/C	- PAIR 9
16	N/C	- PAIR 10
3	N/C	+ PAIR 10
15	N/C	+ PAIR 11
2	N/C	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 21b. Pin assignments for the second (Medium) 26 pins input connector.

SIGNAL INFORMATION

1. DATA (0 – 47) – 48 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
3. SERIAL DATA IN - Serial communications signal going to the camera (Ser TC).
4. SERIAL DATA OUT - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
5. RS232 Rx - Serial communications signal going to the camera (Ser TC)
6. RS232 Tx - Serial communications signal going to the frame grabber (Ser TFG).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected

2.9 MLC – LVDS to Medium Camera Link Converter

MLC is designed to interface any high-resolution digital LVDS camera to any standard Camera Link frame grabber. It converts the standard LVDS (RS644) interface signals to a standard Medium configuration Camera Link output interface – Figure 18. MLC supports 48 data signals, 4 control signals, 8 enable signals, 2 clock signals, and one RS232 serial interface. The maximum data clock is 66 MHz. Figure 19 shows back and front views of the MLC. Table 22 describes the bit assignments for Medium Camera Link interface. Table 23 (a, b) describes the pin assignments for the 100 pin input connectors. Table 24 (a, b) describes the pin assignments for the 26 pin Camera Link output connectors. Detailed views of the LVDS input and Camera link output connectors are shown in Appendix 1.

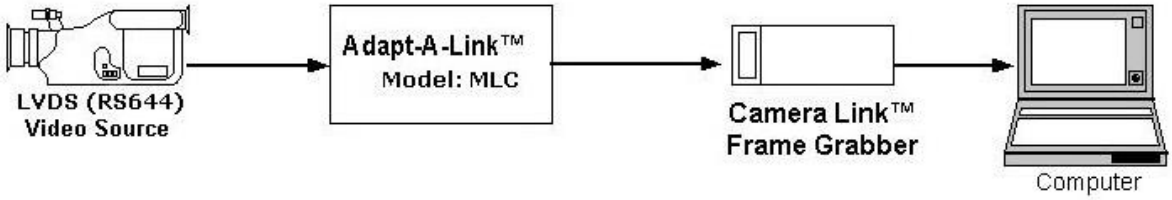

Figure 18. MLC Connectivity.

Figure 19. MLC front (top) and back (bottom) views.

DATA	Port/bit	1/4 Taps 8-bits	1/4 Taps 10-bits	1/4 Taps 12-bits	1/2 Taps 14-bits	1/2 Taps 16-bits	24-bit RGB	30-bit RGB	36-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0	R0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1	R1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2	R2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3	R3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4	R4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5	R5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6	R6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7	R7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0	R8	R8
DATA 9	Port B1	B1	A9	A9	A9	A9	G1	R9	R9
DATA 10	Port B2	B2	nc	A10	A10	A10	G2	N/C	R10
DATA 11	Port B3	B3	nc	A11	A11	A11	G3	N/C	R11
DATA 12	Port B4	B4	B8	B8	A12	A12	G4	B8	B8
DATA 13	Port B5	B5	B9	B9	A13	A13	G5	B9	B9
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6	N/C	B10
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7	N/C	B11
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0	B0	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1	B1	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2	B2	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3	B3	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4	B4	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5	B5	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6	B6	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7	B7	B7
DATA 24	Port D0	D0	D0	D0	B0	B0	N/C	N/C	N/C
DATA 25	Port D1	D1	D1	D1	B1	B1	N/C	N/C	N/C
DATA 26	Port D2	D2	D2	D2	B2	B2	N/C	N/C	N/C
DATA 27	Port D3	D3	D3	D3	B3	B3	N/C	N/C	N/C
DATA 28	Port D4	D4	D4	D4	B4	B4	N/C	N/C	N/C
DATA 29	Port D5	D5	D5	D5	B5	B5	N/C	N/C	N/C
DATA 30	Port D6	D6	D6	D6	B6	B6	N/C	N/C	N/C
DATA 31	Port D7	D7	D7	D7	B7	B7	N/C	N/C	N/C
DATA 32	Port E0	N/C	C0	C0	B8	B8	N/C	G0	G0
DATA 33	Port E1	N/C	C1	C1	B9	B9	N/C	G1	G1
DATA 34	Port E2	N/C	C2	C2	B10	B10	N/C	G2	G2
DATA 35	Port E3	N/C	C3	C3	B11	B11	N/C	G3	G3
DATA 36	Port E4	N/C	C4	C4	B12	B12	N/C	G4	G4
DATA 37	Port E5	N/C	C5	C5	B13	B13	N/C	G5	G5
DATA 38	Port E6	N/C	C6	C6	N/C	B14	N/C	G6	G6
DATA 39	Port E7	N/C	C7	C7	N/C	B15	N/C	G7	G7
DATA 40	Port F0	N/C	C8	C8	N/C	N/C	N/C	G8	G8
DATA 41	Port F1	N/C	C9	C9	N/C	N/C	N/C	G9	G9
DATA 42	Port F2	N/C	N/C	C10	N/C	N/C	N/C	N/C	G10

DATA 43	Port F3	N/C	N/C	C11	N/C	N/C	N/C	N/C	G11
DATA 44	Port F4	N/C	D8	D8	N/C	N/C	N/C	N/C	N/C
DATA 45	Port F5	N/C	D9	D9	N/C	N/C	N/C	N/C	N/C
DATA 46	Port F6	N/C	N/C	D10	N/C	N/C	N/C	N/C	N/C
DATA 47	Port F7	N/C	N/C	D11	N/C	N/C	N/C	N/C	N/C
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
ENABLE 4	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1
ENABLE 5	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1
ENABLE 6	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1
ENABLE 7	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 22. Bit assignments for base Camera Link interface.

SIGNAL INFORMATION

1. ENABLE (0 – 7) – 8 sync signals (usually LVAL, DVAL, FVAL).
2. LVAL - Line Valid is defined HIGH (default) for valid pixels.
3. DVAL - Data Valid is defined HIGH (default) when the data is valid.
4. FVAL - Frame Valid is defined HIGH (default) for valid lines.
5. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
6. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.).

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 0	1	51	+ DATA IN 16
- DATA IN 0	2	52	- DATA IN 16
+ DATA IN 1	3	53	+ DATA IN 17
- DATA IN 1	4	54	- DATA IN 17
+ DATA IN 2	5	55	+ DATA IN 18
- DATA IN 2	6	56	- DATA IN 18
+ DATA IN 3	7	57	+ DATA IN 19
- DATA IN 3	8	58	- DATA IN 19
+ DATA IN 4	9	59	+ DATA IN 20
- DATA IN 4	10	60	- DATA IN 20
+ DATA IN 5	11	61	+ DATA IN 21
- DATA IN 5	12	62	- DATA IN 21
+ DATA IN 6	13	63	+ DATA IN 22
- DATA IN 6	14	64	- DATA IN 22
+ DATA IN 7	15	65	+ DATA IN 23
- DATA IN 7	16	66	- DATA IN 23
+ DATA IN 8	17	67	N/C
- DATA IN 8	18	68	N/C
+ DATA IN 9	19	69	N/C
- DATA IN 9	20	70	N/C
+ DATA IN 10	21	71	N/C
- DATA IN 10	22	72	N/C
+ DATA IN 11	23	73	N/C
- DATA IN 11	24	74	N/C
+ DATA IN 12	25	75	N/C
- DATA IN 12	26	76	N/C
+ DATA IN 13	27	77	N/C
- DATA IN 13	28	78	N/C
+ DATA IN 14	29	79	N/C
- DATA IN 14	30	80	N/C
+ DATA IN 15	31	81	N/C
- DATA IN 15	32	82	N/C
+ CONTROL OUT 0	33	83	N/C
- CONTROL OUT 0	34	84	N/C
+ CONTROL OUT 1	35	85	N/C
- CONTROL OUT 1	36	86	N/C
+ CONTROL OUT 2	37	87	N/C
- CONTROL OUT 2	38	88	N/C
+ CONTROL OUT 3	39	89	N/C
- CONTROL OUT 3	40	90	N/C
+ ENABLE IN 0	41	91	RS232 Rx
- ENABLE IN 0	42	92	RS232 Tx
+ ENABLE IN 1	43	93	SERIAL DATA OUT
- ENABLE IN 1	44	94	SERIAL DATA IN
+ ENABLE IN 2	45	95	+ 6.0 VDC IN
- ENABLE IN 2	46	96	6.0 VDC GROUND
+ ENABLE IN 3	47	97	+ 6.0 VDC IN
- ENABLE IN 3	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN	49	99	GROUND
- PIXEL CLOCK IN	50	100	GROUND

Table 23a. Pin assignments for the first 100 pins input connector.

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 24	1	51	+ DATA IN 40
- DATA IN 24	2	52	- DATA IN 40
+ DATA IN 25	3	53	+ DATA IN 41
- DATA IN 25	4	54	- DATA IN 41
+ DATA IN 26	5	55	+ DATA IN 42
- DATA IN 26	6	56	- DATA IN 42
+ DATA IN 27	7	57	+ DATA IN 43
- DATA IN 27	8	58	- DATA IN 43
+ DATA IN 28	9	59	+ DATA IN 44
- DATA IN 28	10	60	- DATA IN 44
+ DATA IN 29	11	61	+ DATA IN 45
- DATA IN 29	12	62	- DATA IN 45
+ DATA IN 30	13	63	+ DATA IN 46
- DATA IN 30	14	64	- DATA IN 46
+ DATA IN 31	15	65	+ DATA IN 47
- DATA IN 31	16	66	- DATA IN 47
+ DATA IN 32	17	67	N/C
- DATA IN 32	18	68	N/C
+ DATA IN 33	19	69	N/C
- DATA IN 33	20	70	N/C
+ DATA IN 34	21	71	N/C
- DATA IN 34	22	72	N/C
+ DATA IN 35	23	73	N/C
- DATA IN 35	24	74	N/C
+ DATA IN 36	25	75	N/C
- DATA IN 36	26	76	N/C
+ DATA IN 37	27	77	N/C
- DATA IN 37	28	78	N/C
+ DATA IN 38	29	79	N/C
- DATA IN 38	30	80	N/C
+ DATA IN 39	31	81	N/C
- DATA IN 39	32	82	N/C
N/C	33	83	N/C
N/C	34	84	N/C
N/C	35	85	N/C
N/C	36	86	N/C
N/C	37	87	N/C
N/C	38	88	N/C
N/C	39	89	N/C
N/C	40	90	N/C
+ ENABLE IN 4	41	91	N/C
- ENABLE IN 4	42	92	N/C
+ ENABLE IN 5	43	93	N/C
- ENABLE IN 5	44	94	N/C
+ ENABLE IN 6	45	95	+ 6.0 VDC IN
- ENABLE IN 6	46	96	6.0 VDC GROUND
+ ENABLE IN 7	47	97	+ 6.0 VDC IN
- ENABLE IN 7	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN 1	49	99	GROUND
- PIXEL CLOCK IN 1	50	100	GROUND

Table 23b. Pin assignments for the second 100 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- X 0	- PAIR 1
15	+ X 0	+ PAIR 1
3	- X 1	- PAIR 2
16	+ X 1	+ PAIR 2
4	- X 2	- PAIR 3
17	+ X 2	+ PAIR 3
5	- X CLK	- PAIR 4
18	+ X CLK	+ PAIR 4
6	- X 3	- PAIR 5
19	+ X 3	+ PAIR 5
7	+ SerTC	+ PAIR 6
20	- SerTC	- PAIR 6
8	- SerTFG	- PAIR 7
21	+ SerTFG	+ PAIR 7
9	- CC 1	- PAIR 8
22	+ CC 1	+ PAIR 8
10	+ CC 2	+ PAIR 9
23	- CC 2	- PAIR 9
11	- CC 3	- PAIR 10
24	+ CC 3	+ PAIR 10
12	+ CC 4	+ PAIR 11
25	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 24a. Pin assignments for the first (Base) 26 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- Y 0	- PAIR 1
15	+ Y 0	+ PAIR 1
3	- Y 1	- PAIR 2
16	+ Y 1	+ PAIR 2
4	- Y 2	- PAIR 3
17	+ Y 2	+ PAIR 3
5	- Y CLK	- PAIR 4
18	+ Y CLK	+ PAIR 4
6	- Y 3	- PAIR 5
19	+ Y 3	+ PAIR 5
7	N/C	+ PAIR 6
20	N/C	- PAIR 6
8	N/C	- PAIR 7
21	N/C	+ PAIR 7
9	N/C	- PAIR 8
22	N/C	+ PAIR 8
10	N/C	+ PAIR 9
23	N/C	- PAIR 9
11	N/C	- PAIR 10
24	N/C	+ PAIR 10
12	N/C	+ PAIR 11
25	N/C	- PAIR 11
13	Inner Shield	Inner Shield

Table 24b. Pin assignments for the second (Medium) 26 pins output connector.

SIGNAL INFORMATION

1. DATA (0 – 47) – 48 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
3. SERIAL DATA IN - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
4. SERIAL DATA OUT - Serial communications signal going to the camera (Ser TC).
5. RS232 Rx - Serial communications signal going to the frame grabber (Ser TFG)
6. RS232 Tx - Serial communications signal going to the camera (Ser TC).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected.

2.10 MCR – Medium Camera Link to RS422 Converter

MCR is designed to interface any high-resolution digital Camera Link camera to any standard RS422 frame grabber. It converts the standard Medium configuration Camera Link interface signals to a standard RS422 output interface – Figure 20. MCR supports 48 data signals, 4 control signals, 8 enable signals, 2 clock signals, and one RS232 serial interface. The maximum data clock is 33 MHz. Figure 21 shows back and front views of the MCR. Table 25 describes the bit assignments for Medium Camera Link interface. Table 26 (a, b) describes the pin assignments for the 100 pin output connectors. Table 27 (a, b) describes the pin assignments for the 26 pin Camera Link input connectors. Detailed views of the Camera link input and RS422 output connectors are shown in Appendix 1.

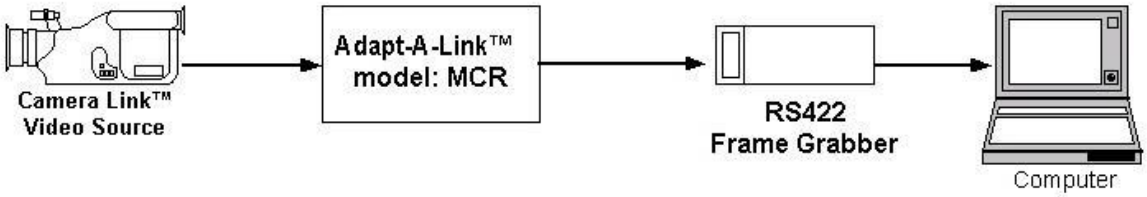

Figure 20. MCR Connectivity.

Figure 21. MCR front (top) and back (bottoms) views.

DATA	Port/bit	1/4 Taps 8-bits	1/4 Taps 10-bits	1/4 Taps 12-bits	1/2 Taps 14-bits	1/2 Taps 16-bits	24-bit RGB	30-bit RGB	36-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0	R0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1	R1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2	R2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3	R3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4	R4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5	R5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6	R6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7	R7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0	R8	R8
DATA 9	Port B1	B1	A9	A9	A9	A9	G1	R9	R9
DATA 10	Port B2	B2	nc	A10	A10	A10	G2	N/C	R10
DATA 11	Port B3	B3	nc	A11	A11	A11	G3	N/C	R11
DATA 12	Port B4	B4	B8	B8	A12	A12	G4	B8	B8
DATA 13	Port B5	B5	B9	B9	A13	A13	G5	B9	B9
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6	N/C	B10
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7	N/C	B11
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0	B0	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1	B1	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2	B2	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3	B3	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4	B4	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5	B5	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6	B6	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7	B7	B7
DATA 24	Port D0	D0	D0	D0	B0	B0	N/C	N/C	N/C
DATA 25	Port D1	D1	D1	D1	B1	B1	N/C	N/C	N/C
DATA 26	Port D2	D2	D2	D2	B2	B2	N/C	N/C	N/C
DATA 27	Port D3	D3	D3	D3	B3	B3	N/C	N/C	N/C
DATA 28	Port D4	D4	D4	D4	B4	B4	N/C	N/C	N/C
DATA 29	Port D5	D5	D5	D5	B5	B5	N/C	N/C	N/C
DATA 30	Port D6	D6	D6	D6	B6	B6	N/C	N/C	N/C
DATA 31	Port D7	D7	D7	D7	B7	B7	N/C	N/C	N/C
DATA 32	Port E0	N/C	C0	C0	B8	B8	N/C	G0	G0
DATA 33	Port E1	N/C	C1	C1	B9	B9	N/C	G1	G1
DATA 34	Port E2	N/C	C2	C2	B10	B10	N/C	G2	G2
DATA 35	Port E3	N/C	C3	C3	B11	B11	N/C	G3	G3
DATA 36	Port E4	N/C	C4	C4	B12	B12	N/C	G4	G4
DATA 37	Port E5	N/C	C5	C5	B13	B13	N/C	G5	G5
DATA 38	Port E6	N/C	C6	C6	N/C	B14	N/C	G6	G6
DATA 39	Port E7	N/C	C7	C7	N/C	B15	N/C	G7	G7

DATA 40	Port F0	N/C	C8	C8	N/C	N/C	N/C	G8	G8
DATA 41	Port F1	N/C	C9	C9	N/C	N/C	N/C	G9	G9
DATA 42	Port F2	N/C	N/C	C10	N/C	N/C	N/C	N/C	G10
DATA 43	Port F3	N/C	N/C	C11	N/C	N/C	N/C	N/C	G11
DATA 44	Port F4	N/C	D8	D8	N/C	N/C	N/C	N/C	N/C
DATA 45	Port F5	N/C	D9	D9	N/C	N/C	N/C	N/C	N/C
DATA 46	Port F6	N/C	N/C	D10	N/C	N/C	N/C	N/C	N/C
DATA 47	Port F7	N/C	N/C	D11	N/C	N/C	N/C	N/C	N/C
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
ENABLE 4	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1
ENABLE 5	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1
ENABLE 6	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1
ENABLE 7	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 25. Bit assignments for Medium Camera Link interface.

SIGNAL INFORMATION

7. ENABLE (0 – 7) – 8 sync signals (usually LVAL, DVAL, FVAL).
8. LVAL - Line Valid is defined HIGH (default) for valid pixels.
9. DVAL - Data Valid is defined HIGH (default) when the data is valid.
10. FVAL - Frame Valid is defined HIGH (default) for valid lines.
11. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
12. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.).

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 0	50	100	+ DATA OUT 16
- DATA OUT 0	49	99	- DATA OUT 16
+ DATA OUT 1	48	98	+ DATA OUT 17
- DATA OUT 1	47	97	- DATA OUT 17
+ DATA OUT 2	46	96	+ DATA OUT 18
- DATA OUT 2	45	95	- DATA OUT 18
+ DATA OUT 3	44	94	+ DATA OUT 19
- DATA OUT 3	43	93	- DATA OUT 19
+ DATA OUT 4	42	92	+ DATA OUT 20
- DATA OUT 4	41	91	- DATA OUT 20
+ DATA OUT 5	40	90	+ DATA OUT 21
- DATA OUT 5	39	89	- DATA OUT 21
+ DATA OUT 6	38	88	+ DATA OUT 22
- DATA OUT 6	37	87	- DATA OUT 22
+ DATA OUT 7	36	86	+ DATA OUT 23
- DATA OUT 7	35	85	- DATA OUT 23
+ DATA OUT 8	34	84	N/C
- DATA OUT 8	33	83	N/C
+ DATA OUT 9	32	82	N/C
- DATA OUT 9	31	81	N/C
+ DATA OUT 10	30	80	N/C
- DATA OUT 10	29	79	N/C
+ DATA OUT 11	28	78	N/C
- DATA OUT 11	27	77	N/C
+ DATA OUT 12	26	76	N/C
- DATA OUT 12	25	75	N/C
+ DATA OUT 13	24	74	N/C
- DATA OUT 13	23	73	N/C
+ DATA OUT 14	22	72	N/C
- DATA OUT 14	21	71	N/C
+ DATA OUT 15	20	70	N/C
- DATA OUT 15	19	69	N/C
+ CONTROL IN 0	18	68	N/C
- CONTROL IN 0	17	67	N/C
+ CONTROL IN 1	16	66	N/C
- CONTROL IN 1	15	65	N/C
+ CONTROL IN 2	14	64	N/C
- CONTROL IN 2	13	63	N/C
+ CONTROL IN 3	12	62	N/C
- CONTROL IN 3	11	61	N/C
+ ENABLE OUT 0	10	60	RS232 Tx
- ENABLE OUT 0	9	59	RS232 Rx
+ ENABLE OUT 1	8	58	SERIAL DATA IN
- ENABLE OUT 1	7	57	SERIAL DATA OUT
+ ENABLE OUT 2	6	56	+ 6.0 VDC OUT
- ENABLE OUT 2	5	55	6.0 VDC GROUND
+ ENABLE OUT 3	4	54	+ 6.0 VDC OUT
- ENABLE OUT 3	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT	2	52	GROUND
- PIXEL CLOCK OUT	1	51	GROUND

Table 26a. Pin assignments for the first 100 pins output connector.

SIGNAL	PIN	PIN	SIGNAL
+ DATA OUT 24	50	100	+ DATA OUT 40
- DATA OUT 24	49	99	- DATA OUT 40
+ DATA OUT 25	48	98	+ DATA OUT 41
- DATA OUT 25	47	97	- DATA OUT 41
+ DATA OUT 26	46	96	+ DATA OUT 42
- DATA OUT 26	45	95	- DATA OUT 42
+ DATA OUT 27	44	94	+ DATA OUT 43
- DATA OUT 27	43	93	- DATA OUT 43
+ DATA OUT 28	42	92	+ DATA OUT 44
- DATA OUT 28	41	91	- DATA OUT 44
+ DATA OUT 29	40	90	+ DATA OUT 45
- DATA OUT 29	39	89	- DATA OUT 45
+ DATA OUT 30	38	88	+ DATA OUT 46
- DATA OUT 30	37	87	- DATA OUT 46
+ DATA OUT 31	36	86	+ DATA OUT 47
- DATA OUT 31	35	85	- DATA OUT 47
+ DATA OUT 32	34	84	N/C
- DATA OUT 32	33	83	N/C
+ DATA OUT 33	32	82	N/C
- DATA OUT 33	31	81	N/C
+ DATA OUT 34	30	80	N/C
- DATA OUT 34	29	79	N/C
+ DATA OUT 35	28	78	N/C
- DATA OUT 35	27	77	N/C
+ DATA OUT 36	26	76	N/C
- DATA OUT 36	25	75	N/C
+ DATA OUT 37	24	74	N/C
- DATA OUT 37	23	73	N/C
+ DATA OUT 38	22	72	N/C
- DATA OUT 38	21	71	N/C
+ DATA OUT 39	20	70	N/C
- DATA OUT 39	19	69	N/C
N/C	18	68	N/C
N/C	17	67	N/C
N/C	16	66	N/C
N/C	15	65	N/C
N/C	14	64	N/C
N/C	13	63	N/C
N/C	12	62	N/C
N/C	11	61	N/C
+ ENABLE OUT 4	10	60	N/C
- ENABLE OUT 4	9	59	N/C
+ ENABLE OUT 5	8	58	N/C
- ENABLE OUT 5	7	57	N/C
+ ENABLE OUT 6	6	56	+ 6.0 VDC OUT
- ENABLE OUT 6	5	55	6.0 VDC GROUND
+ ENABLE OUT 7	4	54	+ 6.0 VDC OUT
- ENABLE OUT 7	3	53	6.0 VDC GROUND
+ PIXEL CLOCK OUT 1	2	52	GROUND
- PIXEL CLOCK OUT 1	1	51	GROUND

Table 26b. Pin assignments for the second 100 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- X 0	- PAIR 1
12	+ X 0	+ PAIR 1
24	- X 1	- PAIR 2
11	+ X 1	+ PAIR 2
23	- X 2	- PAIR 3
10	+ X 2	+ PAIR 3
22	- X CLK	- PAIR 4
9	+ X CLK	+ PAIR 4
21	- X 3	- PAIR 5
8	+ X 3	+ PAIR 5
20	+ SerTC	+ PAIR 6
7	- SerTC	- PAIR 6
19	- SerTFG	- PAIR 7
6	+ SerTFG	+ PAIR 7
18	- CC 1	- PAIR 8
5	+ CC 1	+ PAIR 8
17	+ CC 2	+ PAIR 9
4	- CC 2	- PAIR 9
16	- CC 3	- PAIR 10
3	+ CC 3	+ PAIR 10
15	+ CC 4	+ PAIR 11
2	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 27a. Pin assignments for the first (Base) 26 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
25	- Y 0	- PAIR 1
12	+ Y 0	+ PAIR 1
24	- Y 1	- PAIR 2
11	+ Y 1	+ PAIR 2
23	- Y 2	- PAIR 3
10	+ Y 2	+ PAIR 3
22	- Y CLK	- PAIR 4
9	+ Y CLK	+ PAIR 4
21	- Y 3	- PAIR 5
8	+ Y 3	+ PAIR 5
20	N/C	+ PAIR 6
7	N/C	- PAIR 6
19	N/C	- PAIR 7
6	N/C	+ PAIR 7
18	N/C	- PAIR 8
5	N/C	+ PAIR 8
17	N/C	+ PAIR 9
4	N/C	- PAIR 9
16	N/C	- PAIR 10
3	N/C	+ PAIR 10
15	N/C	+ PAIR 11
2	N/C	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 27b. Pin assignments for the second (Medium) 26 pins input connector.

SIGNAL INFORMATION

1. DATA (0 – 47) – 48 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
3. SERIAL DATA IN - Serial communications signal going to the camera (Ser TC).
4. SERIAL DATA OUT - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
5. RS232 Rx - Serial communications signal going to the camera (Ser TC)
6. RS232 Tx - Serial communications signal going to the frame grabber (Ser TFG).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected

2.11 MRC – RS422 to Medium Camera Link Converter

MRC is designed to interface any high-resolution digital RS422 camera to any standard Camera Link frame grabber. It converts the standard RS422 interface signals to a standard Medium configuration Camera Link output interface – Figure 22. MRC supports 48 data signals, 4 control signals, 8 enable signals, 2 clock signals, and one RS232 serial interface. The maximum data clock is 33 MHz. Figure 23 shows back and front views of the MRC. Table 28 describes the bit assignments for Medium Camera Link interface. Table 29 (a, b) describes the pin assignments for the 100 pin input connectors. Table 30 (a, b) describes the pin assignments for the 26 pin Camera Link output connectors. Detailed views of the RS422 input and Camera link output connectors are shown in Appendix 1.

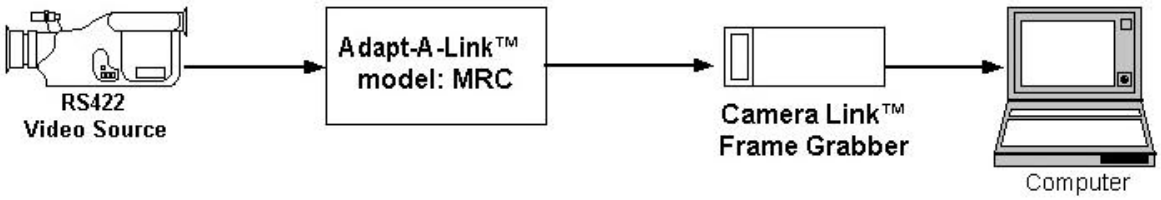

Figure 22. MRC Connectivity.

Figure 23. MRC front (top) and back (bottom) views.

DATA	Port/bit	1/4 Taps 8-bits	1/4 Taps 10-bits	1/4 Taps 12-bits	1/2 Taps 14-bits	1/2 Taps 16-bits	24-bit RGB	30-bit RGB	36-bit RGB
DATA 0	Port A0	A0	A0	A0	A0	A0	R0	R0	R0
DATA 1	Port A1	A1	A1	A1	A1	A1	R1	R1	R1
DATA 2	Port A2	A2	A2	A2	A2	A2	R2	R2	R2
DATA 3	Port A3	A3	A3	A3	A3	A3	R3	R3	R3
DATA 4	Port A4	A4	A4	A4	A4	A4	R4	R4	R4
DATA 5	Port A5	A5	A5	A5	A5	A5	R5	R5	R5
DATA 6	Port A6	A6	A6	A6	A6	A6	R6	R6	R6
DATA 7	Port A7	A7	A7	A7	A7	A7	R7	R7	R7
DATA 8	Port B0	B0	A8	A8	A8	A8	G0	R8	R8
DATA 9	Port B1	B1	A9	A9	A9	A9	G1	R9	R9
DATA 10	Port B2	B2	nc	A10	A10	A10	G2	N/C	R10
DATA 11	Port B3	B3	nc	A11	A11	A11	G3	N/C	R11
DATA 12	Port B4	B4	B8	B8	A12	A12	G4	B8	B8
DATA 13	Port B5	B5	B9	B9	A13	A13	G5	B9	B9
DATA 14	Port B6	B6	N/C	B10	N/C	A14	G6	N/C	B10
DATA 15	Port B7	B7	N/C	B11	N/C	A15	G7	N/C	B11
DATA 16	Port C0	C0	B0	B0	N/C	N/C	B0	B0	B0
DATA 17	Port C1	C1	B1	B1	N/C	N/C	B1	B1	B1
DATA 18	Port C2	C2	B2	B2	N/C	N/C	B2	B2	B2
DATA 19	Port C3	C3	B3	B3	N/C	N/C	B3	B3	B3
DATA 20	Port C4	C4	B4	B4	N/C	N/C	B4	B4	B4
DATA 21	Port C5	C5	B5	B5	N/C	N/C	B5	B5	B5
DATA 22	Port C6	C6	B6	B6	N/C	N/C	B6	B6	B6
DATA 23	Port C7	C7	B7	B7	N/C	N/C	B7	B7	B7
DATA 24	Port D0	D0	D0	D0	B0	B0	N/C	N/C	N/C
DATA 25	Port D1	D1	D1	D1	B1	B1	N/C	N/C	N/C
DATA 26	Port D2	D2	D2	D2	B2	B2	N/C	N/C	N/C
DATA 27	Port D3	D3	D3	D3	B3	B3	N/C	N/C	N/C
DATA 28	Port D4	D4	D4	D4	B4	B4	N/C	N/C	N/C
DATA 29	Port D5	D5	D5	D5	B5	B5	N/C	N/C	N/C
DATA 30	Port D6	D6	D6	D6	B6	B6	N/C	N/C	N/C
DATA 31	Port D7	D7	D7	D7	B7	B7	N/C	N/C	N/C
DATA 32	Port E0	N/C	C0	C0	B8	B8	N/C	G0	G0
DATA 33	Port E1	N/C	C1	C1	B9	B9	N/C	G1	G1
DATA 34	Port E2	N/C	C2	C2	B10	B10	N/C	G2	G2
DATA 35	Port E3	N/C	C3	C3	B11	B11	N/C	G3	G3
DATA 36	Port E4	N/C	C4	C4	B12	B12	N/C	G4	G4
DATA 37	Port E5	N/C	C5	C5	B13	B13	N/C	G5	G5
DATA 38	Port E6	N/C	C6	C6	N/C	B14	N/C	G6	G6

DATA 39	Port E7	N/C	C7	C7	N/C	B15	N/C	G7	G7
DATA 40	Port F0	N/C	C8	C8	N/C	N/C	N/C	G8	G8
DATA 41	Port F1	N/C	C9	C9	N/C	N/C	N/C	G9	G9
DATA 42	Port F2	N/C	N/C	C10	N/C	N/C	N/C	N/C	G10
DATA 43	Port F3	N/C	N/C	C11	N/C	N/C	N/C	N/C	G11
DATA 44	Port F4	N/C	D8	D8	N/C	N/C	N/C	N/C	N/C
DATA 45	Port F5	N/C	D9	D9	N/C	N/C	N/C	N/C	N/C
DATA 46	Port F6	N/C	N/C	D10	N/C	N/C	N/C	N/C	N/C
DATA 47	Port F7	N/C	N/C	D11	N/C	N/C	N/C	N/C	N/C
ENABLE 0	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
ENABLE 1	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
ENABLE 2	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
ENABLE 3	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
ENABLE 4	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1	LVAL1
ENABLE 5	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1	FVAL1
ENABLE 6	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1	DVAL1
ENABLE 7	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C
CONTROL 0	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1	CC 1
CONTROL 1	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2	CC 2
CONTROL 2	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3	CC 3
CONTROL 3	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4	CC 4

Table 28. Bit assignments for base Camera Link interface.

SIGNAL INFORMATION

7. ENABLE (0 – 7) – 8 sync signals (usually LVAL, DVAL, FVAL).
8. LVAL - Line Valid is defined HIGH (default) for valid pixels.
9. DVAL - Data Valid is defined HIGH (default) when the data is valid.
10. FVAL - Frame Valid is defined HIGH (default) for valid lines.
11. LVAL, DVAL and FVAL can be independently inverted with a set of jumpers located inside the box. Please contact Imperx for more information.
12. CONTROL (0 – 3) – 4 control signals (usually trigger, integration, etc.).

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 0	1	51	+ DATA IN 16
- DATA IN 0	2	52	- DATA IN 16
+ DATA IN 1	3	53	+ DATA IN 17
- DATA IN 1	4	54	- DATA IN 17
+ DATA IN 2	5	55	+ DATA IN 18
- DATA IN 2	6	56	- DATA IN 18
+ DATA IN 3	7	57	+ DATA IN 19
- DATA IN 3	8	58	- DATA IN 19
+ DATA IN 4	9	59	+ DATA IN 20
- DATA IN 4	10	60	- DATA IN 20
+ DATA IN 5	11	61	+ DATA IN 21
- DATA IN 5	12	62	- DATA IN 21
+ DATA IN 6	13	63	+ DATA IN 22
- DATA IN 6	14	64	- DATA IN 22
+ DATA IN 7	15	65	+ DATA IN 23
- DATA IN 7	16	66	- DATA IN 23
+ DATA IN 8	17	67	N/C
- DATA IN 8	18	68	N/C
+ DATA IN 9	19	69	N/C
- DATA IN 9	20	70	N/C
+ DATA IN 10	21	71	N/C
- DATA IN 10	22	72	N/C
+ DATA IN 11	23	73	N/C
- DATA IN 11	24	74	N/C
+ DATA IN 12	25	75	N/C
- DATA IN 12	26	76	N/C
+ DATA IN 13	27	77	N/C
- DATA IN 13	28	78	N/C
+ DATA IN 14	29	79	N/C
- DATA IN 14	30	80	N/C
+ DATA IN 15	31	81	N/C
- DATA IN 15	32	82	N/C
+ CONTROL OUT 0	33	83	N/C
- CONTROL OUT 0	34	84	N/C
+ CONTROL OUT 1	35	85	N/C
- CONTROL OUT 1	36	86	N/C
+ CONTROL OUT 2	37	87	N/C
- CONTROL OUT 2	38	88	N/C
+ CONTROL OUT 3	39	89	N/C
- CONTROL OUT 3	40	90	N/C
+ ENABLE IN 0	41	91	RS232 Rx
- ENABLE IN 0	42	92	RS232 Tx
+ ENABLE IN 1	43	93	SERIAL DATA OUT
- ENABLE IN 1	44	94	SERIAL DATA IN
+ ENABLE IN 2	45	95	+ 6.0 VDC IN
- ENABLE IN 2	46	96	6.0 VDC GROUND
+ ENABLE IN 3	47	97	+ 6.0 VDC IN
- ENABLE IN 3	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN	49	99	GROUND
- PIXEL CLOCK IN	50	100	GROUND

Table 29a. Pin assignments for the first 100 pins input connector.

SIGNAL	PIN	PIN	SIGNAL
+ DATA IN 24	1	51	+ DATA IN 40
- DATA IN 24	2	52	- DATA IN 40
+ DATA IN 25	3	53	+ DATA IN 41
- DATA IN 25	4	54	- DATA IN 41
+ DATA IN 26	5	55	+ DATA IN 42
- DATA IN 26	6	56	- DATA IN 42
+ DATA IN 27	7	57	+ DATA IN 43
- DATA IN 27	8	58	- DATA IN 43
+ DATA IN 28	9	59	+ DATA IN 44
- DATA IN 28	10	60	- DATA IN 44
+ DATA IN 29	11	61	+ DATA IN 45
- DATA IN 29	12	62	- DATA IN 45
+ DATA IN 30	13	63	+ DATA IN 46
- DATA IN 30	14	64	- DATA IN 46
+ DATA IN 31	15	65	+ DATA IN 47
- DATA IN 31	16	66	- DATA IN 47
+ DATA IN 32	17	67	N/C
- DATA IN 32	18	68	N/C
+ DATA IN 33	19	69	N/C
- DATA IN 33	20	70	N/C
+ DATA IN 34	21	71	N/C
- DATA IN 34	22	72	N/C
+ DATA IN 35	23	73	N/C
- DATA IN 35	24	74	N/C
+ DATA IN 36	25	75	N/C
- DATA IN 36	26	76	N/C
+ DATA IN 37	27	77	N/C
- DATA IN 37	28	78	N/C
+ DATA IN 38	29	79	N/C
- DATA IN 38	30	80	N/C
+ DATA IN 39	31	81	N/C
- DATA IN 39	32	82	N/C
N/C	33	83	N/C
N/C	34	84	N/C
N/C	35	85	N/C
N/C	36	86	N/C
N/C	37	87	N/C
N/C	38	88	N/C
N/C	39	89	N/C
N/C	40	90	N/C
+ ENABLE IN 4	41	91	N/C
- ENABLE IN 4	42	92	N/C
+ ENABLE IN 5	43	93	N/C
- ENABLE IN 5	44	94	N/C
+ ENABLE IN 6	45	95	+ 6.0 VDC IN
- ENABLE IN 6	46	96	6.0 VDC GROUND
+ ENABLE IN 7	47	97	+ 6.0 VDC IN
- ENABLE IN 7	48	98	6.0 VDC GROUND
+ PIXEL CLOCK IN 1	49	99	GROUND
- PIXEL CLOCK IN 1	50	100	GROUND

Table 29b. Pin assignments for the second 100 pins input connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- X 0	- PAIR 1
15	+ X 0	+ PAIR 1
3	- X 1	- PAIR 2
16	+ X 1	+ PAIR 2
4	- X 2	- PAIR 3
17	+ X 2	+ PAIR 3
5	- X CLK	- PAIR 4
18	+ X CLK	+ PAIR 4
6	- X 3	- PAIR 5
19	+ X 3	+ PAIR 5
7	+ SerTC	+ PAIR 6
20	- SerTC	- PAIR 6
8	- SerTFG	- PAIR 7
21	+ SerTFG	+ PAIR 7
9	- CC 1	- PAIR 8
22	+ CC 1	+ PAIR 8
10	+ CC 2	+ PAIR 9
23	- CC 2	- PAIR 9
11	- CC 3	- PAIR 10
24	+ CC 3	+ PAIR 10
12	+ CC 4	+ PAIR 11
25	- CC 4	- PAIR 11
13	Inner Shield	Inner Shield
26	Inner Shield	Inner Shield

Table 30a. Pin assignments for the first (Base) 26 pins output connector.

PIN	Camera Link Signal	Signal Name
1	Inner Shield	Inner Shield
14	Inner Shield	Inner Shield
2	- Y 0	- PAIR 1
15	+ Y 0	+ PAIR 1
3	- Y 1	- PAIR 2
16	+ Y 1	+ PAIR 2
4	- Y 2	- PAIR 3
17	+ Y 2	+ PAIR 3
5	- Y CLK	- PAIR 4
18	+ Y CLK	+ PAIR 4
6	- Y 3	- PAIR 5
19	+ Y 3	+ PAIR 5
7	N/C	+ PAIR 6
20	N/C	- PAIR 6
8	N/C	- PAIR 7
21	N/C	+ PAIR 7
9	N/C	- PAIR 8
22	N/C	+ PAIR 8
10	N/C	+ PAIR 9
23	N/C	- PAIR 9
11	N/C	- PAIR 10
24	N/C	+ PAIR 10
12	N/C	+ PAIR 11
25	N/C	- PAIR 11
13	Inner Shield	Inner Shield

Table 30b. Pin assignments for the second (Medium) 26 pins output connector.

SIGNAL INFORMATION

1. DATA (0 – 47) – 48 bit actual data.
2. PIXEL CLOCK - Reference camera clock (X CLK). Maximum frequency is 66 MHz.
3. SERIAL DATA IN - Serial communications signal going to the frame grabber (Ser TFG). SERIAL DATA IN/OUT are 3.3V LVTTL level signals.
4. SERIAL DATA OUT - Serial communications signal going to the camera (Ser TC).
5. RS232 Rx - Serial communications signal going to the frame grabber (Ser TFG)
6. RS232 Tx - Serial communications signal going to the camera (Ser TC).
7. RS232 Tx/Rx and SERIAL DATA IN/OUT are mutually exclusive. The serial interface can be switched from RS232 (default) to SERIAL DATA with a set of jumpers located inside the box. **Units sold prior to October 1, 2004 do not support RS232 interface.** Please contact Imperx for more information.
8. 6.0 VDC OUT - Provides power (if needed) for the next Adapt-A-Link unit, if two or more adapter units are used in the same chain. Each unit can provide 1000 mA MAX.
9. 6.0 VDC GROUND - Ground return from the next Adapt-A-Link unit in the chain.
10. N/C – not used, not connected.

Chapter 3 – Adapt-A-Link Warranty

Adapt-A-Link Warranty

This chapter discusses the adapters' warranty and operating instructions.

3.1 OPERATING INSTRUCTIONS

Each unit is fully tested before shipping. If for some reason the unit is not operational after power up please check the following:

1. Check the power supply and all I/O cables. Make sure that all the connectors are firmly attached. Verify the proper input/out cable connection.
2. Check the green LED and verify that is steady ON.
3. If the unit generates an output signal but image is corrupted or unstable check the cables and make sure they are firmly attached.
4. If the unit has power, but there is no output signal, check the cable pin mapping and the polarity of the enable signals.
5. If you still have problems with the unit operation, please contact technical support:
   Email: techsupport@imperx.com
   Toll Free (866) 849-1662 or (+1) 561-989-0006
   Fax: (+1) 561-989-0045
   Visit our Web Site: www.imperx.com

3.2 WARRANTY

Imperx warrants performance of its products and related software to the specifications applicable at the time of sale in accordance with Imperx's standard warranty, which is 1 (one) year parts and labor. Do not open the box of the unit. Warranty voids if the unit has been open or tampered.

IMPORTANT NOTICE

The adapters hve been tested and complies with the limits of Class A digital device, pursuant to part 15 of the FCC rules.

Imperx reserves the right to make changes to its products or to discontinue any product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

IMPERX PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Appendix 1– Cables and Connectors

Cables and Connectors

This appendix provides a quick reference to the cables and connectors used in Adapt-A-Link family Adapters

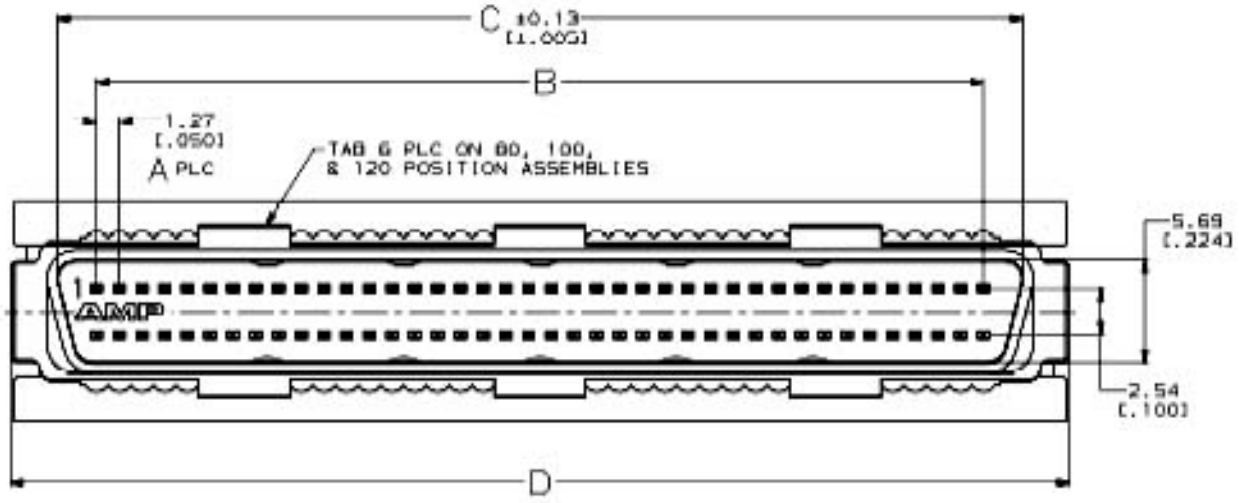

Figure 24. 100 pin male cable plug - TYCO/AMP # 749111-8.
B = 62.23 mm, C = 66.60 mm, D = 71.86 mm.
Back shell kit TYCO/AMP # 749081-1

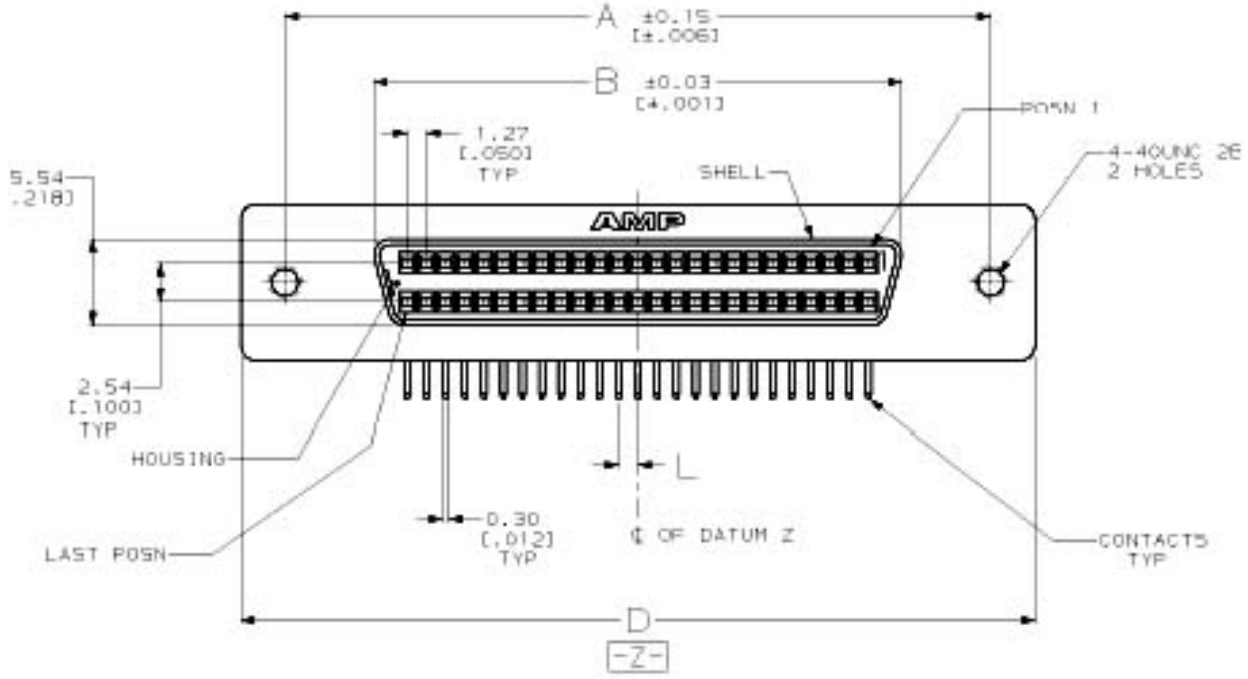

Figure 25. 100 pin female box jack - TYCO/AMP # 787169-9.
A = 78.23 mm, B = 66.45 mm, D = 84.20 mm

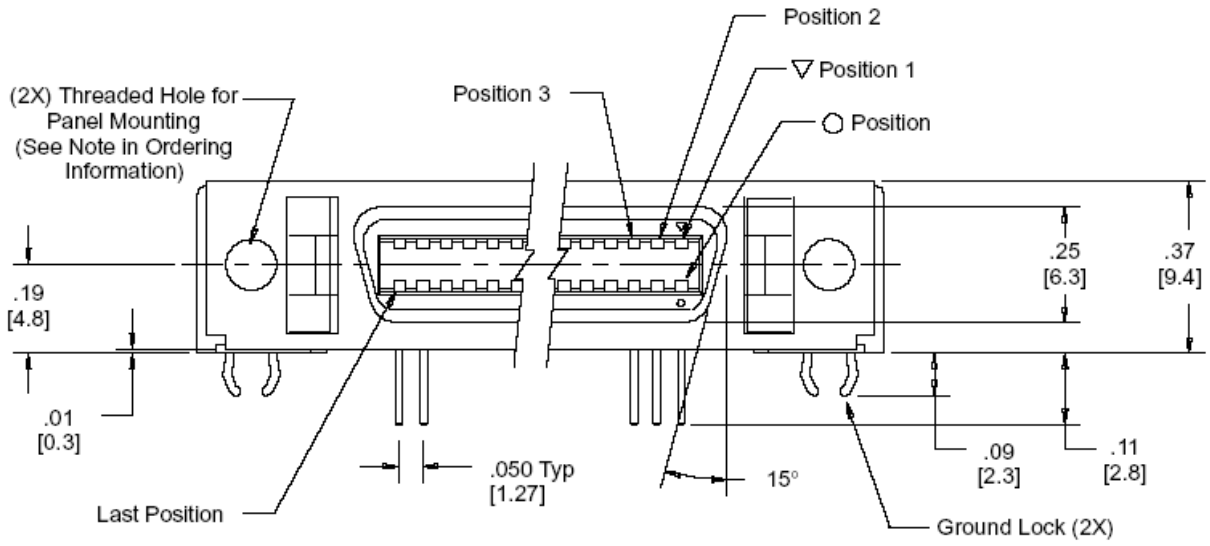

Figure 26. 26 pins Camera Link female box jack – 3M-10226-55G3VC.

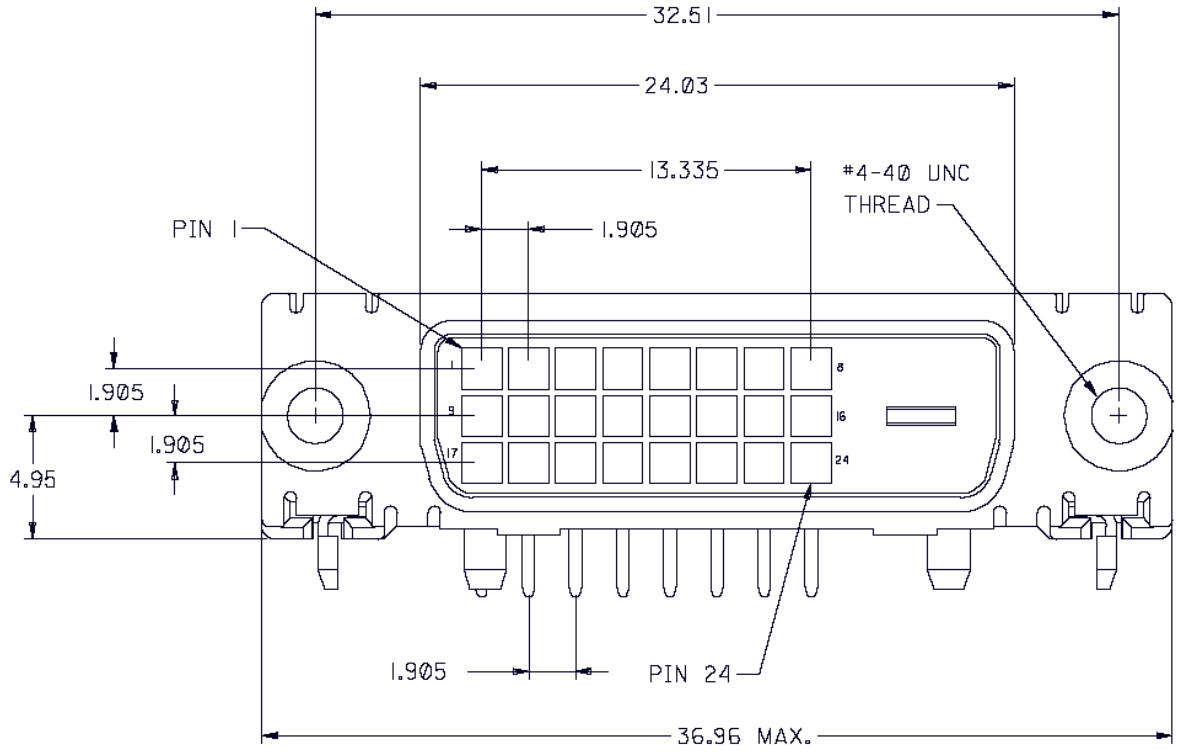

Figure 27. 24 pins DVI female box jack – DVI-D, Molex.